ELE301: Digital Design with FPGAs
Spring 2018 Schedule

Instructor: Professor Jien-Chung Lo
Schneider, X-42996, jcl@ele.uri.edu or jclce@uri.edu

Class Webpage: http://www.ele.uri.edu/Courses/ele301/
Textbook: J. C. Lo, "Modern Digital Designs with EDA, VHDL and FPGA," Terasic, 2015.

Lecture: MWF 11--11:50, Pastore Hall 234
Office Hours: TuTh 12--2 and We 1--2 Schneider

Schedule

wk	Lecture	Lecture Topics (Tentative)	Tests
1	1/22,24,26	Chapter 1: Introduction & Chapter 2: VHDL Primers	
2	1/29,31, 2/2	Chapter 2: VHDL/Quartus/FPGA introduction	
3	2/5,7,9	Chapter 3: RTL Digital Designs	HW #1
4	2/12,13,16	Chapter 4: Design of Digital Systems	Test #1
5	2/21,23	Chapter 4: Design of Digital Systems	
6	2/26,28, 3/2	Chapter 6: VGA timing, Video memory, Animation	HW #2
7	3/5,7,9	Supplement: MTL2 LCD display	Test #2
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8	3/19,21,23	Chapter 7: Text Video, bitmap fonts	
9	3/26,28,30	Supplement: MTL2 Touch sensor, VerilogHDL	HW #3
10	4/2,4,6	Chapter 8: Audio Codec, I2C	Test #3
11	4/9,11,13	Chapter 8: Digital Audio, Synthesizer	
12	4/16,18,20	Chapter 7: Multi-Colored Displays	HW #4
13	4/23,25,27	Chapter 9: Advanced Examples/Chapter 10: VHDL	Test #4
14	4/30	Supplement: DE1-SoC vs. DE10-nano	
	Final Exam: Friday May 4, 11:30AM - 2:30AM		

Grading Policy:

Homework	4 x 8% =	32%
Tests:	4 x 10% =	40%
Final Exam (Project) : 26%		
Final project technical merits		12%
Final project report		10%
Final project presentation		4%

ELE301/302 Overview

In this class, you are expected to master the followings:

1. **VHDL**: The IEEE standard hardware description language.
2. **FPGA**: Field programmable gate array. We are now using the Altera's products.
3. **RTL** (register-transfer level) logic designs: in which you are designing logic circuits with higher level modules or blocks, as opposite to using primitive gates, i.e., as in ELE202.
4. **ASM** (algorithmic state machine): The approach to design finite state machines directly from algorithms-like flow charts.
5. Optionally, we may cover **Verilog HDL**, the second IEEE standard hardware description language.

Students are expected to already have basic knowledge and skills in digital logic designs. Also necessary is the laboratory skills from ELE302, the laboratory component of ELE301. Software programming skill may help but is not required. Students are expected to spend about 5 to 6 hours outside the classroom and laboratory hours per week for ELE301 and ELE302. This is a normal level of effort consistent with the University rule.

The ABET outcomes for are:

- Critically evaluate and compare the results from different alternatives in each laboratory assignment (l).
- Ability to evaluate the trade-offs in digital design selections and to make decisions based on various considerations using modern EDA tools. (e,k,l)
- Ability to design, simulate, synthesize and verify complex digital systems with synthesis tools. (b)
- Ability to design specifications for a digital system and then design a digital system that meets the specifications. (c)
- Perform six laboratory exercises and assignments covering a wide range of potential applications including human interface, control, communication, etc. (c,k)

For students with special needs:

Any student with a documented disability is welcome to contact me early in the semester so that we may work out reasonable accommodations to support your success in this course. The grading policy will remain the same as stated above. One should also contact Disability Services for Students, Office of Student Life, 330 Memorial Union, 874-2098.

ELE302: Electronic Design Automation Laboratory
Spring 2018 Schedule

Instructor: Professor Jien-Chung Lo
Schneider, X-42996, jcl@ele.uri.edu or jclce@uri.edu
Teaching Assistants: Mustafa Cavus
SAKAI: Laboratory materials are available on ELE301 Sakai site
Labs (ELE302 sections 1 to 4): Tu We Th Mo 2:15 - 5:00 PM Schneider 200I

Schedule

Laboratories	L01 (Tu)	L02 (We)	L03 (Th)	L04 (Mo)
Lab 0: Preparations	1/23	1/24	1/25	1/22
Lab 1: Quartus and VHDL primer	1/30	1/31	2/1	1/29
Lab 2: Adders and Multipliers	2/6	2/7	2/8	2/5
Lab 3: Frequency Counter	2/13	2/14	2/15	2/12
Lab 4: Sequence Detection	2/20	2/21	2/22	2/26
Lab 5: Stopwatch/Pedometer	2/27	2/28	3/1	3/5
Lab 6: VGA/Racquetball	3/6	3/7	3/8	3/19
Lab 7: Bitmap Fonts and Sprites	3/20	3/21	3/22	3/26
Lab 8: MTL2 Touch/Morse Code	3/27	3/28	3/29	4/2
Lab 9: Synthesizer	4/3	4/4	4/5	4/9
Project: Classical video game	4/10,17,24	4/11,18,25	4/12,19, 26	4/16,23,30

Grading Policy:

Lab 1 to Lab9: 9 x 9% =	81%
Final Project =	19%

Grading rubric:
Lab report pages, at the end of each lab handout, are filled and handed in before leaving the lab.

10 - 9: complete all works; no or minor bug
8 - 7: complete all works; more than minor bugs
6 - 5: complete most (3/4) works; some bugs in the completed parts
4 - 3: complete half (1/2) of the works
2 - 1: complete some (1/4) works
0: no work; no show; no excuse