ELE306 Spring2008 LAB4

RTL Viewer, etc.

The purpose of this lab is to guide you through the use of RTL view and other features in Quartus II that might help in understand how VHDL got map onto FPGA.

Exercise

- Open Lab3b from exercise#2 of Lab3.
- Generate RTL schematic by "Tools → Netlist Viewers → RTL Viewer"
- A screen should show the RTL schematic of lab3b design on the right and a directory-like hierarchical tree on the left pane.
- In the schematic view, light-green boxes are components used in the VHDL. Double click on these boxes will bring you a lower-level view. (Use the back or forward button to navigate; these are the two last buttons on the tool bar at left)
- Expand the hierarchical tree on the left and examine in turn the instances (the components declared and used; each instances has its own hierarchical tree), primitives (primitive function blocks used, such as adder, flip-flops, etc.), pins (those inputs and outputs declared in the entity) and nets (all internal signals). When double click on the selected signal, the display will automatically changed to show the signal in the tree and in schematic.
- Highlight the keyboard module (turn red) and then right click. You will see eight possible "Locate in …" choices. The six choices available to us are: Assignment Editor, Design File, Chip Planner(Floorplan & Chip Editor), Resource Property Editor, Technology Map Viewer and Timing Closure Floorplan. Try the first two: (a) in Assignment Editor, you will not see anything useful as the component is embedded; and (b) the VHDL editor will pop-up and the line where keyboard module was instantiated will be located. You may try this will other signals or modules. Note that not all options will be available for any signal.
- If you choose Timing Closure Floorplan (or by "Assignments → Timing Closure Floorplan), the Timing Closure viewer will pop-up. The main window of this viewer shows the floorplan of the FPGA. You will see how the blocks inside the Flex10K70 exactly as they should be inside the IC. Here are the statistics:
    - 3,744 LEs (logic elements; each with a 4-input Look-Up Table (LUT) and a D-Flip-Flop, and other auxiliary circuitry).
    - 468 LABs (Logic array block; each with 8 Les and is shown as a block with 8 segments in the floorplan viewer). These 468 LABs are arranged in two 26X9 planes separated by the EABs.
    - 9 EABs (Embedded array block; each is a RAM with 2Kbits and can be arranged as 256X8, 512X4, 1024X2 or 2048X1). These 9 EABs are in the center column.
    - Maximum user I/O pins 189 out of 240 (associated with IOE: I/O element).

- Three windows are shown at the lower part. They show the inputs (fan-in), the Boolean equation(s), and the outputs (fan-out) of the highlighted block.
- Note that RTL and floorplan viewer works only after full compilation. As the compilation is completed, the compilation report will be showing. (For a completed project, you may see the compilation report from the Processing menu)
- There are five major sections showing on the left panel: Generic summary (Legal notice, flow summary, flow setting, flow elapsed time), Analysis & Synthesis, Fitter, Assembler, and Timing Analyzer. The first part is a quick summary of compilation results, as shown on the main window on the right:
    - How many LEs (logic elements) in Flex10K70 are used?
    - How many pins are used in this design?
    - How many memory bits (in EAB's) are still available?
- Analysis & Synthesis: the first step of compilation is to translate your VHDL codes into Boolean functions and then optimized them. There are six reports in this category. Pay special attention to "Analysis & Synthesis Equations" section. In the equations, the following symbols are used: $ is XOR, & is AND, # is OR and ! is NOT.
- Fitter: The second step is to decompose the Boolean functions so the decomposed functions can fit into the fixed sized logic elements (LE's), and thus the name fitter. This step is usually the most time consuming (can be seen from the "Flow Elapsed Time" under the generic reports. This is because of the need to find the best combination of LE's to implement user's circuits. There are eight categories under this section:
    - Fitter summary is almost always identical to the Flow summary earlier.
    - Fitter Settings: These are the compilation options chosen.
    - Fitter Device Options: options available when fitting device.
    - Fitter Equations: This should list the equations after the decomposition.
    - Floorplan View: will show you the same floorplan view.
    - Resources Section: A detailed run downs of how resources were allocated.
    - Pin-Out File: This is the file generated by the Fitter to be used for the Assembler in the next step. You can see how the pins are specified.
    - Fitter Messages: messages.
- Assembler: Generating the Hex file that contains the device programming information, to be downloaded to the FPGA in the programming step. Two files are generated: SRAM Object File (.sof) and Programmer Object File (.pof). The programmer download .sof to the FPGA; Flex10k70 is SRAM-based.
- Timing Analyzer: The last step is to verify the timing information of your design (this can only be done after it is fitted to FPGA). You may define a delay time goal for your design and this step will help you verify that goal.

Assignment

- Perform the above steps with your Lab3 assignment #3 design.

Lab 4 Report

- RTL view and compilation report from assignment.