ELE306: Electronic Design Automation Laboratory
Spring 2008 Schedule

Instructor: Professor Jien-Chung Lo
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Class Webpage: http://www.ele.uri.edu/Courses/ele306
Textbook: P. J. Ashenden, The Designer's Guide to VHDL, 2nd ed., Morgan Kaufmann Pub. ISBN 1-55860-674-2

Lecture: TuTh 11--12:15, Kelley 102
Labs: L01: M 2--4:45, L02: Tu 2-4:45, L04: Th 2-4:45 Kelley 220
Office Hours: TuTh 12:30-2 Kelley A-221

Schedule

wk	Lecture	L01	L02	L04	Laboratory Topics	Tests
1	1/24	-	-	-		
2	1/29,31			1/31 (1)		
3	2/5,7	2/4	2/5	2/7 (2)	Lab 1: Schematic entry	
4	2/12,14	2/11	2/12	2/14 (2)	Lab 2: Hierarchical VHDL Designs	
5	2/19,21	2/18	2/19	2/21 (3)	Lab 2	test#1
6	2/26,28	2/25	2/26	2/28 (3)	Lab 3: VGA and PS/2: design reuse	
7	3/4,6	3/3	3/4	3/6 (5)	Lab 3	
8	3/11,13	3/10	3/11	3/13 (5)	Lab 4: Chip Editor	
9	-	-	-	-	Spring Break	
10	3/25,27	3/24	3/25	3/27 (4)	Lab 5: Algorithmic State Machines	
11	4/1,3	3/31	4/1	4/3 (6)	Lab 5	test#2
12	4/8,10	4/7	4/8	4/10 (p1)	Lab 6: Serial Communication	
13	4/15,17	4/14	4/15	4/17 (p2)	Project week 1	
14	4/22,24	4/21	4/22	4/24 (p3)	Project week 2	
15	4/29	4/28	4/29	-	Project week 3	
	5/6 11:30AM-2:30PM at K220				Project Presentation at Final Exam	

Grading Policy:
Lab 1 (1 wk) --- 5% Lab 2 (2 wk) --- 10%
Lab 3 (2 wk) --- 10% Lab 4 (1 wk) --- 5%
Lab 5 (2 wk) --- 10% Lab 6 (1 wk) --- 5%
Proj (3 wk) --- 25% (Demo – 5%, Report --- 10%, Presentation --- 10%)
Tests: 2X15% = 30%

ELE306 Overview

In this class, you are expected to master the followings:

1. **VHDL**: The IEEE standard hardware description language.
2. **FPGA**: Field programmable gate array. We are now using the Altera's products.
3. **RTL** (register-transfer level) logic designs: in which you are designing logic circuits with higher level modules or blocks, as opposite to using primitive gates, i.e., as in ELE202.
4. **ASM** (algorithmic state machine): The approach to design finite state machines directly from algorithms-like flow charts.
5. Optionally, we may cover **Verilog HDL**, the second IEEE standard hardware description language.

Students are expected to have basic knowledge and skills in digital logic designs. Also necessary is the laboratory skills. Programming skill may help but is not required. Students are expected to spend about 5 to 6 hours outside the classroom and laboratory hours per week for this class. This is a normal level of effort consistent with the University rule.

Project milestones and rubrics:

The project milestones and rubrics will be handed out in the class. The project should be done in ten progressively difficult steps; each step will earn 10% of the baseline grade. This baseline grade will then be used in calculating your score for the project.

The ABET outcomes for this course are:

- Critically evaluate and compare the results from different alternatives in each laboratory assignment (l).
- Ability to evaluate the trade-offs in digital design selections and to make decisions based on various considerations using modern EDA tools. (e,k,l)
- Ability to design, simulate, synthesize and verify complex digital systems with synthesis tools. (b)
- Ability to design specifications for a digital system and then design a digital system that meets the specifications. (c)
- Perform six laboratory exercises and assignments covering a wide range of potential applications including human interface, control, communication, etc. (c,k)

For students with special needs:

Any student with a documented disability is welcome to contact me early in the semester so that we may work out reasonable accommodations to support your success in this course. The grading policy will remain the same as stated above. One should also contact Disability Services for Students, Office of Student Life, 330 Memorial Union, 874-2098.