ELE307 Spring2009 LAB5

What's new in this lab:

VHDL	Generic map, custom library.
EDA	Altera's megafunction.
FPGA	PLL, built-in memory array.
RTL	Complex timing signal generation, memory interface.

Exercise

- Download lab5_1.qar from ftp://ele.uri.edu/outgoing/jcl/306/lab5_1.qar.
- Restore, and compile the project. Program the DE2 board.
- This exercise gives you a VGA circuit (vga.vhd) that assumes a resolution of 160x120 with 3-bit for color for each pixel. Use Switches 17-10 for X (line 112 of lab5_1.vhd), switches 9-3 for Y (line 113 of lab5_1.vhd), and switches 2-0 for colors (line 122 of lab5_1.vhd). After you have set up the X and Y coordinates and the color, hit KEY(3) to write it to the video RAM. States b4 to b6 (lines 127-135) represent the three steps to write to the Video RAM. The color is the data written to Video RAM and will show up on HEX3 and HEX2.
- Set up the X and Y coordinates and hit KEY(2) will read the contents of that particular location in the Video RAM. The data (or color) will be displayed on HEX1 and HEX0.
- The DE2 board's VGA interface has a 10-bit DAC for each color. Since we only use 3 bits for each pixel, each bit is mapped to all 10 bits (lines 107 to 109 of vga.vhd).
- Lines 116 to 126 of vga.vhd instantiate the Altera's megafunction "altpll". The CycloneII FPGA on the DE2 board has four built-in PLLs. We use this PLL to generate the pixel clock for the VGA timing. The pixel clock is generated as 50MHz * 65/128 (lines 117 and 118 of vga.vhd).
- Lines 72 and 73 of vga.vhd describe how the Video RAM address is generated from the horizontal and vertical timing. Note that the Video RAM has two independent ports (lines 39 to 58 in vga.vhd). PortA is operated on "pclock", the pixel clock, and is used to continuously provide screen displays according to the contents of the Video RAM. PortB is operated on "clock" and is used for the main circuit to read or write to the same Video RAM.
- For the report, show your calculation for the total of memory bits used here. Verify this number with that shown on the compilation report (print out the compilation report too).
- Use "Chip Planner" to see how these memory bits are allocated. Note the dark green regions. Also, the four PLLs are located at the four corners. The one used here is marked in dark brown.

Assignment (lab5_2)

- Create a circuit that allow user to paint on the screen. You will need to add the keyboard.
- The current paint brush/pen location is indicated by a "cursor". You may use a simple white or any color block, or even blinking one to represent the "cursor."
- Use the "arrow keys" on the keyboard to move the cursor around the screen. You should detect when the cursor is going out of bound and prevent it from happening.
- Use "space bar" on the keyboard to switch between paint and no-paint mode.
- Use number keys (0 to 7) on the keyboard to decide the color.
- When moving cursor (without painting) through already painted area, whatever already been painted there should be preserved. This is accomplished by reading from the Video RAM and saving the video data before moving cursor to that position; and to restore that video data after the cursor moves away.

Lab 5 Report:

Title page: Lab title, section number, your name, student ID and email address.

The body of your report should include a one paragraph introduction. Descriptions of your experiences from the exercise parts which associated with the items required below. The following required items should be embedded with the text explanation not aggregated at the end of your report. Approaches and thinking behind your solution to the assignment. Lesson learned from this lab.

From the Exercise:

1. Printout of the compilation report (flow summary).
2. Show your formula and calculations for the total memory usage in exercise lab5_1.
3. In reference to the state machine SV in lab5_1.vhd, draw timing diagrams for read and write operations of Video RAM, respectively.

From the Assignment:

4. Algorithm or flowchart of your paint circuit.
5. VHDL listing.

Also, send the followings to TA:

1. Lab5_2.qar (assignment)