ELE307 Spring2009 LAB7

What's new in this lab:

VHDL	Type conversion.
EDA	Memory Initialization File editor, instances in RTL Viewer.
FPGA	Built-in memory array as ROM.
RTL	ROM, character generation ROM, conversion lookup table.

Exercise#1

- Download lab7_1.qar from ftp://ele.uri.edu/outgoing/jcl/306/lab7_1.qar.
- Restore, and compile the project. Program the DE2 board.
- This exercise gives you a VGA circuit (vga.vhd) that assumes a resolution of 640x320 with 1-bit for color for each pixel. Line 86 of vga.vhd describe how a temporary address is generated from the horizontal and vertical timing. Be aware that this vga.vhd is different from that in lab5 and lab6!
- Lines 61 to 72 of this vga.vhd show the character ROM or "font_table" holding patterns for all upper-case letters and numbers, and some symbols. The ROM size is 512x8 for 64 8x8 characters or patterns. Double click on the "tcgrom.mif" on the file list will bring out the memory initialization file editor. You should see how the character font is formed.
- Lines 125 to 127 show how to convert std_logic_vector to integer to be used as the index for the array. The function "conv_integer" is available in the package "std_logic_arith".
- Use switches 17 downto 12 to set up X, and switches 11 downto 6 for Y. Use switches 5 downto 0 to select character (in ASCII code). Hit KEY(3) to write the character to the Video RAM and thus show the character on screen. Note that the screen size is now 80x60 characters; each character is 8x8 pixels.
- In RTL Viewer, expand "instances" in the "Hierarchy List" on the left. Double click on "vga" will bring up the view of component "vga" described in "vga.vhd". Expand the instances again and you will see PLL, font_table and video_memory. Single click on the name (not double click) will center view on the component. Use this as clue to draw a schematic (for the report) of how Video RAM and Character ROM (font_table) are connected in the design.

Exercise#2

- Download lab7_2.qar from ftp://ele.uri.edu/outgoing/jcl/306/lab7_2.qar.
- Restore, and compile the project. Program the DE2 board.
- This exercise does not have the VGA. Instead it shows how to convert the "scan_code" from PS/2 keyboard to the standard ASCII code. Actually, the simplified ROM (k2a.mif) in this exercise only converts upper case letters and numbers.
- Lines 37 to 49 are the declaration of this lookup table or ROM. Line 41 is commented out. When activate, this generic map item will remove the register at the ROM output. By default, the input address and output are both registered.

- The state machine KEYIN was designed to pick up only the scan_code when a key is first hit. This is accomplished by detecting the pattern "F0". If "F0" occurs two bytes before the new code, then th is a new "make code" and thus become the "new_scan_code" (line 82).
- The signal "code_buf" is a FIFO designed to hold three bytes from the keyboard. This provides the necessary depth for the above examination.

Assignment (lab7_3)

- Create a simple terminal demo: whatever you type on the keyboard will show up on the VGA (text) screen. This might be limited to no shift or control key and to only those supported by the conversion ROM or lookup table.
- Starting from the upper left corner, the character typed in will be displayed from left to right. At the end of each line (80 characters per line), the next character should appear on the far left of the next line.
- "Enter" or ASCII "0D" will immediately advance to the far left of the next line.
- When reached to the last line (60 lines total), and a new line is needed, the entire screen should be scrolled up by one line.

Lab 7 Report:

Title page: Lab title, section number, your name, student ID and email address.

The body of your report should include a one paragraph introduction. Descriptions of your experiences from the exercise parts which associated with the items required below. The following required items should be embedded with the text explanation not aggregated at the end of your report. Approaches and thinking behind your solution to the assignment. Lesson learned from this lab.

From the Exercise #1:

1. Draw a schematic of how Video RAM and Character ROM (font_table) are connected in the design. Also show the segment(s) of VHDL code that correspond to the schematic.

From the Exercise #2:

2. None.

From the Assignment:

3. Algorithm or flowchart.
4. VHDL listing.

Also, send the followings to TA:

1. Lab7_3.qar (assignment)