ELE306: Electronic Design Automation
Spring 2009 Schedule

Instructor: Professor Jien-Chung Lo
Kelley Annex 221, X-42996, jcl@ele.uri.edu

Class Webpage: http://www.ele.uri.edu/Courses/ele306/s09
Textbook: P. J. Ashenden, The Student's Guide to VHDL, 2nd ed.,
Morgan Kaufmann Pub. ISBN: 978-1-55860-865-8

Lecture: TuTh 11--12:15, Kelley 102
Labs(ELE307): L02: Tu 2--4:45, L03: We 2-4:45, L04: Th 2-4:45 Kelley 220
Office Hours: TuWeTh 1-2 Kelley A-221

Schedule

wk	Lecture	Lecture Topics	Tests
1	1/22	Introduction and overview	
2	1/27,29	VHDL: modeling, data types (ch 1 & 2)	
3	2/3,5	VHDL: operations (ch 2) FPGA: structure	
4	2/10,12	EDA: functional and timing simulations	Test#1
5	2/17,19	VHDL: Sequential statements (ch 3)	
6	2/24,26	VHDL: Composite data types and operations (ch 4)	
7	3/3,5	RTL: PS/2 interface	Mid-Term
8	3/10,12	VHDL: Basic Modeling Constructs (ch 5)	
9	---	--------Spring Break----------	
10	3/24,26	RTL: Algorithm State Machine	
11	3/31, 4/2	RTL: VGA and video RAM	
12	4/7,9	RTL: serial communication (RS-232)	
13	4/14,16	VHDL: subprograms (ch 6)	Test#2
14	4/21,23	VHDL: standard packages (ch 9) EDA: Altera's library	
15	4/28	EDA & FPGA: synthesis and mapping, JTAG	
	Final Exam May 8, 3-6PM		

Grading Policy:

Homework:	4 X 5% = 20%
Tests:	2 X 15% = 30%
Mid-Term:	20%
Final Exam:	30%

ELE306/307 Overview

In this class, you are expected to master the followings:

1. **VHDL**: The IEEE standard hardware description language.
2. **FPGA**: Field programmable gate array. We are now using the Altera's products.
3. **RTL** (register-transfer level) logic designs: in which you are designing logic circuits with higher level modules or blocks, as opposite to using primitive gates, i.e., as in ELE202.
4. **ASM** (algorithmic state machine): The approach to design finite state machines directly from algorithms-like flow charts.
5. Optionally, we may cover **Verilog HDL**, the second IEEE standard hardware description language.

Students are expected to have basic knowledge and skills in digital logic designs. Also necessary is the laboratory skills for ELE307, the laboratory component of ELE306. Programming skill may help but is not required. Students are expected to spend about 5 to 6 hours outside the classroom and laboratory hours per week for ELE307. This is a normal level of effort consistent with the University rule.

The ABET outcomes for are:

- Critically evaluate and compare the results from different alternatives in each laboratory assignment (l).
- Ability to evaluate the trade-offs in digital design selections and to make decisions based on various considerations using modern EDA tools. (e,k,l)
- Ability to design, simulate, synthesize and verify complex digital systems with synthesis tools. (b)
- Ability to design specifications for a digital system and then design a digital system that meets the specifications. (c)
- Perform six laboratory exercises and assignments covering a wide range of potential applications including human interface, control, communication, etc. (c,k)

For students with special needs:

Any student with a documented disability is welcome to contact me early in the semester so that we may work out reasonable accommodations to support your success in this course. The grading policy will remain the same as stated above. One should also contact Disability Services for Students, Office of Student Life, 330 Memorial Union, 874-2098.

ELE307: Electronic Design Automation Laboratory
Spring 2009 Schedule

Instructor: Professor Jien-Chung Lo
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Teaching Assistant: Will Simoneau
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Schedule

Laboratories	**L02**	**L03**	**L04**
Lab 0: Preparations	-	-	-
Lab 1: New project and import assignments	2/3	1/28	1/29
Lab 2: Clock signals and frequency generator	2/10	2/4	2/2
Lab 3: PS/2 keyboard interface	2/17	2/11	2/12
Lab 4: Multiple finite state machines	2/24	2/25	2/19
Lab 5: VGA video interface	3/3	3/4	2/26
Lab 6: Multi-port Video RAM	3/10	3/11	3/5
Lab 7: Text and graphic video display	3/24	3/25	3/12
Lab 8: Serial communication, RS-232	3/31	4/1	3/26
Lab 9: Sprites and animation	4/7.14	4/8,15	4/2,9
Lab 10: Video game with serial communication	4/21,28	4/22,29	4/16,23

Grading Policy:

Labs 1 ~ 8 are one-week labs. Students will take turn serve as the lead. Each student will lead exactly four times and received grades for no more than four labs as leader. Each lab is 15% of the total grade: 12% to the leader and 3% for the non-leader.

Labs 9 and 10 are two weeks teamed labs, with 20% of total grade each lab.