Charge Coupled Device

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History

A Charge-Coupled Device is an analog shift register, enabling the electric charges, as the form of analog signal, to be transferred through successive stages under the control of an appropriate clock signal. Willard Boyle and George E. Smith invented it in 1969 at AT&T Bell labs. The objective of the design was to transfer charge along the surface of a semiconductor. "As the CCD started its life as a memory device, one could only "inject" charge into the device at an input register. However, it was immediately clear that the CCD could receive charge via the photoelectric effect and electronic images could be created. This use is so predominant that in common parlance, "CCD" is (erroneously) used as a synonym for a type of image sensor even though, strictly speaking, "CCD" refers solely to the way that the image signal is read out from the chip."[2]

Basics of operation

The early CCD is based on MOS that is similar to other MOS devices. Fig.1 shows a CCD shift

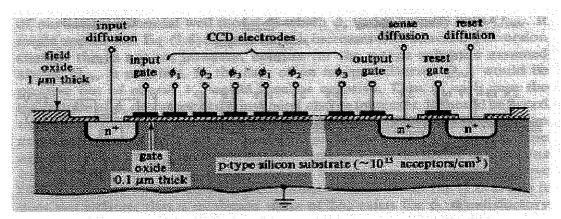


Fig.1 CCD as a shift register [1]

register. The charges are injected electrically from input. When gate voltage is higher than substrate voltage, the electric field associated will pull the free electrons from the p-substrate to the top of semiconductor material (near the oxide surface) and form a depletion region with negative charge. The width of this depletion region is related to the voltage level applied on the gate. This depletion region can be used as a potential well to store charge carriers.

As extra charges are injected from the input electrode, the input gate and the gate adjacent to it (gate1) are biased appropriately such that injected charges will be transferred to gate1. By applying a proper clocks in phase 1 through 3, the charges will transferred gate by gate to the

Architecture

Imaging CCD can be implemented in one dimensional, as in bar code reader or two dimensional, as in digital camera. Fig.5 shows a one dimensional CCD architecture.

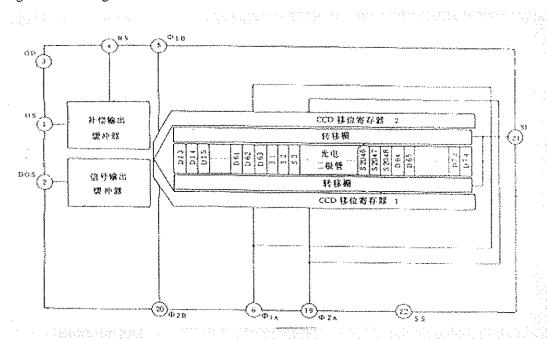


Fig.5 CCD array architecture [4]

Three most common architectures of two-dimensional CCD are full-frame, frame-transfer and interline as shown in Fig.6. In full-frame architecture, a mechanical shutter is open in optical integration mode and closed in charge transfer mode. The charge transfer procedure is shown in Fig.7.

Common Charge-Coupled Device (CCD) Architectures Interline Transfer Full-Frame Frame Transfer lmaging Array **Parallel** Parallel imaging Register Shift Direction **Parallel** Storage Register Storage **Output Node** Serial Shift Direction Serial Régister Figure 7

Fig.6 CCD architectures

In frame-transfer architecture, only half of the device area is open to object and a high reflective

Microlens Array Interline CCD Technology

light sensitivity (due to light scattering) and dynamic range. The solution is to use micro-lens on the top of each photodiode as shown in Fig.8.

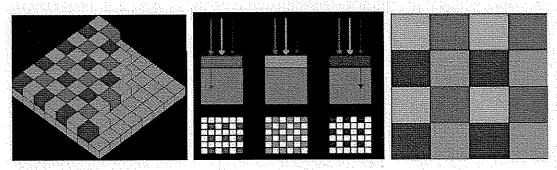
Microlens Exposure Gate Light Photodiode Photodiode Photodiode Photodiode Integrated Electrons Overflow Drain Figure 8

Color CCD

Fig.8 Micro-lens to increase the light sensitivity

So far all the CCDs we mentioned can only

sensor the gray-ness, or light intensity. In another word, they are black-and-white CCD. In order to receive color image a few of techniques have been invented. The first one is filtering and most popular filter is Bayer filter as shown in Fig.9. The image pixels is arranged to form interlaced grids. One fourth of the cells are used for blue light sensor and another one fourth for red light. The rest half of them are used for green light (Human eye is most sensitive to green). The image is then interpolated using a demosaicing algorithm. Sony adopts another combination of color filter, RGBE filter, for its



(a) Bayer filter and its working diagram

(b) RGBE filter

Fig. 9 Bayer filter and RGBE filter

Cybershot camera [2].

Foveon X3 sensor is based on the silicon color absorption chart as shown in Fig.10, using an array of

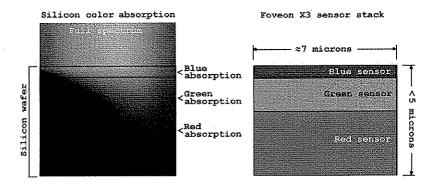


Fig.10 Foveon sensor

Appendix:

Process [1]

The photoactive region of the CCD is, generally, an <u>epitaxial</u> layer of silicon. It has a doping of p+ (Boron) and is grown upon the <u>substrate</u> material, often p++. In buried channel devices, the type of design utilized in most modern CCDs, certain areas of the surface of the silicon are ion implanted with phosphorus, giving them an n-doped designation. This region defines the channel in which the photo-generated charge packets will travel. The gate oxide, i.e. the capacitor dielectric, is grown on top of the epitaxial layer and substrate. Later on in the process polysilicon gates are deposited by <u>chemical vapor deposition</u>, patterned with <u>photolithography</u>, and etched in such a way that the separately phased gates lie perpendicular to the channels. The channels are further defined by utilization of the LOCOS process to produce the channel stop region. Channel stops are thermally grown oxides that serve to isolate the charge packets in one column from those in another. These channel stops are produced before the <u>polysilicon</u> gates are, as the LOCOS process utilizes a high temperature step that would destroy the gate material. The channels stops are parallel to, and exclusive of, the channel, or "charge carrying", regions. Channel stops often have a p+ doped region underlying them, providing a further barrier to the electrons in the charge packets (this discussion of the physics of CCD devices assumes an electron transfer device, though hole transfer is possible).