PCM Encoding and Decoding:

Aim:

Introduction to PCM encoding and decoding.

Introduction:

PCM Encoding:

The input to the PCM ENCODER module is an analog message. This must be constrained to a defined bandwidth and amplitude range.

The maximum allowable message bandwidth will depend upon the sampling rate to be used. The Nyquist criterion must be observed.

The amplitude range must be held within the $\pm$ 2.0 volts range of the TIMS ANALOG REFERENCE LEVEL. This is in keeping with the input amplitude limits set for all analog modules.

A step-by-step description of the operation of the module follows:

1. the module is driven by an external TTL clock.

2. the input analog message is *sampled* periodically. The *sample rate* is determined by the external clock.

3. the sampling is a *sample-and-hold* operation. It is internal to the module, and cannot be viewed by the user . What is held is the *amplitude* of the analog message *at the sampling instant*.

4. each sample amplitude is compared with a finite set of amplitude levels. These are distributed (uniformly, for *linear* sampling) within the range $\pm$ 2.0 volts (the TIMS ANALOG REFERENCE LEVEL). These are the system *quantizing* levels.

5. each quantizing level is assigned a *number*, starting from zero for the lowest (most negative) level, with the highest number being (L-1), where L is the available number of levels.

6. each sample is *assigned* a digital (binary) code word representing the number associated with the quantizing level which is closest to the sample amplitude. The number of bits 'n' in the digital code word will depend upon the number of quantizing levels. In fact, $n = \log_2(L)$.

7. the code word is *assembled into a time frame* together with other bits as may be required (described below). In the TIMS PCM ENCODER (and many commercial systems) a single extra bit is added, in the least significant bit position. This is alternately a *one* or a *zero*. These bits are used by subsequent
decoders for frame synchronization.

8. the *frames* are transmitted serially. They are transmitted at the same rate as the samples are taken. The serial bit stream appears at the output of the module.

9. also available from the module is a synchronizing signal FS ('frame synch'). This signals the *end* of each data frame.

The PCM Ecoder Module:
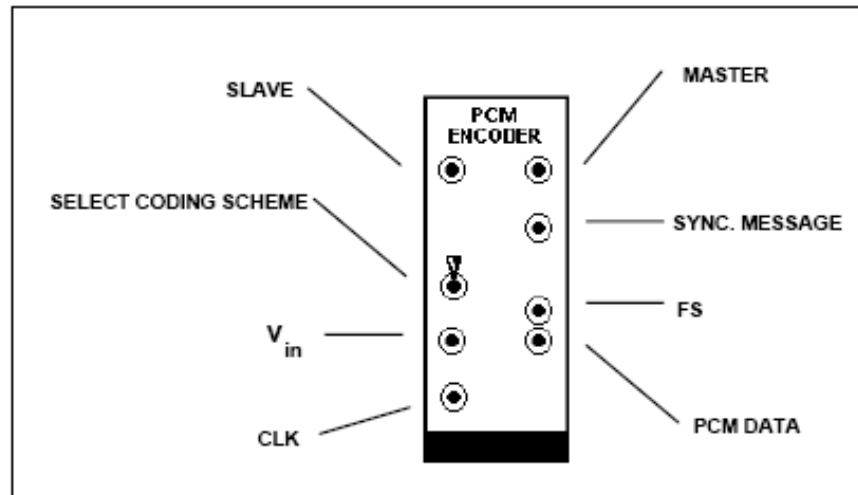
Front panel layout of the PCM ENCODER

Note and understand the purpose of each of the input and output connections, and the three-position toggle switch. Counting from the top, these are:

- *SLAVE*: not used during this experiment. Do *not* connect anything to this input.

- *MASTER*: not used during this experiment. Do *not* connect anything to this output.

- *SYNC. MESSAGE:* periodic, 'synchronized', message. Either sinusoidal, or sinusoidal-like ('sinuous'), its frequency being a sub-multiple of the MASTER CLOCK (being any one of four frequencies selected by an on-board switch SW2). A message synchronized to the system clock is convenient for obtaining stable oscilloscope displays. Having a recognisable shape (but being more complex than a simple sine wave) gives a qualitative idea of distortion during the decoding process (examined in a later experiment). See Table A-1 in the Appendix to this experiment for more details.

- *SELECT CODING SCHEME:* a three-position toggle switch which selects the 4-bit or 7-bit encoding scheme of the analog samples; or (together with an onboard jumper connection) the companding scheme.

- *FS*: frame synchronization, a signal which indicates the end of each data frame.

- *Vin::* the analog signal to be encoded.

- *PCM DATA*: the output data stream, the examination of which forms the major part of this experiment.

- **CLK**: this is a TTL (red) input, and serves as the MASTER CLOCK for the module. Clock rate must be 10 kHz or less. For this experiment you will use the 8.333 kHz TTL signal from the MASTER SIGNALS module.

The TIMS PCM time frame:

Each binary word is located in a *time frame*. The time frame contains eight *slots* of equal length, and is eight clock periods long. The slots, from first to last, are numbered 7 through 0. These slots contain the bits of a binary word. The least significant bit (LSB) is contained in slot 0. The LSB consists of alternating *ones* and *zeros*. These are placed ('embedded') in the frame by the encoder itself, and cannot be modified by the user. They are used by subsequent decoders to determine the location of each frame in the data stream,
and its length. The remaining seven slots are available for the bits of the binary code word. Thus the system is capable of a resolution of seven-bits maximum. This resolution, for purposes of experiment, can be reduced to four bits (by front panel switch). The 4- bit mode uses only five of the available eight slots - one for the embedded frame synchronization bits, and the remaining four for the binary code word (in slots 4, 3, 2, and 1).

Experimental Procedure:

T1 select the TIMS companding A$_4$-law with the on-board COMP jumper (in preparation for a later part of the experiment).

T2 locate the on-board switch SW2. Put the LEFT HAND toggle DOWN and the RIGHT HAND toggle UP. This sets the frequency of a message from the module at SYNC. MESSAGE. This message is synchronized to a submultiple of the MASTER CLOCK frequency.

Patching Up:

To determine some of the properties of the analog to digital conversion process it is best to start with a DC message. This ensures completely stable oscilloscope displays, and enables easy identification of the quantizing levels.

Selecting the 4-bit encoding scheme reduces the number of levels (2^4) to be examined.

T3 insert the module into the TIMS frame. Switch the front panel toggle switch to 4-BIT LINEAR (ie., no companding).

T4 patch the 8.333 kHz TTL SAMPLE CLOCK from the MASTER SIGNALS module to the CLK input of the PCM ENCODER module.

T5 connect the V$_{in}$ input socket to ground of the variable DC module.

T6 connect the frame synchronization signal FS to the oscilloscope ext. synch. input.

*T7 on CH1-A display the frame synchronization signal FS. Adjust the sweep speed to show three frame markers. These mark the **end** of each frame.*

T8 on CH2-A display the CLK signal.

T9 record the number of clock periods per frame.

Currently the analog input signal is zero volts (V_{in} is grounded). Before checking with the oscilloscope, consider what the PCM output signal might look like. Make a sketch of this signal, fully annotated. Then:

T10 on CH2-B display the PCM DATA from the PCM DATA output socket.

Except for the alternating pattern of '1' and '0' in the frame marker slot, you might have expected nothing else in the frame (all zeros), because the input analog signal is at zero volts. But you do not now the coding scheme.
There *is* an analog *input* signal to the encoder. It is of zero volts. This will have been coded into a 4-bit binary *output* number, which will appear in *each* frame. It need not be '0000'. The *same* number appears in *each* frame because the analog input is *constant*.
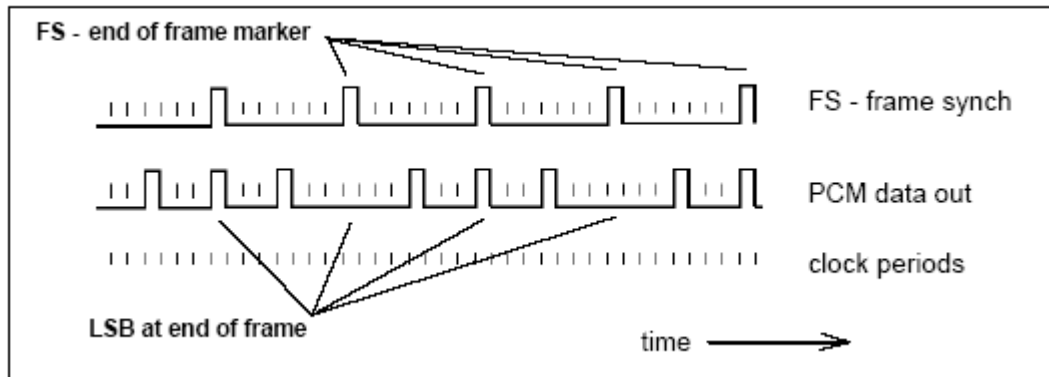
5 frames of 4-bit PCM output for zero amplitude input

Knowing:

1. the number of slots per frame is 8
2. the location of least significant bit is coincident with the end of the frame
3. the binary word length is four bits
4. the first three slots are 'empty' (in fact filled with zeros, but these remain unchanged under all conditions of the 4-bit coding scheme)

T11 identify the binary word in slots 4, 3, 2, and 1.

Quantizing levels for 4-bit linear encoding:

You will now proceed to determine the quantizing/encoding scheme for the 4-bit linear case.

T12 remove the ground connection, and connect the output of the VARIABLE DC module to V_{in}. Sweep the DC voltage slowly backwards and forwards over its complete range, and note how the data pattern changes in discrete jumps.

T13 *use the oscilloscope (CH1-B) to monitor the DC amplitude at V_{in} . Adjust V_{in} to its maximum negative value. Record the DC voltage and the pattern of the 4-bit binary number.*

T14 *slowly increase the amplitude of the DC input signal until there is a sudden change to the PCM output signal format. Record the format of the new digital word, and the input amplitude at which the change occurred.*

T15 *continue this process over the full range of the DC supply.*

T16 *draw a diagram showing the quantizing levels and their associated binary numbers.*

4-bit data format

From measurements made so far you should be able to answer the questions:
- what is the sampling rate ?
- what is the frame width ?
- what is the width of a data bit ?
- what is the width of a data word ?
- how many quantizing levels are there ?
- are the quantizing levels uniformly (linearly) spaced ?

7-bit linear encoding

T17 *change to 7-bit linear encoding by use of the front panel toggle switch.*

T18 *make sufficient measurements so that you can answer all of the above questions in the section titled **4-bit data format** above.*

Companding:

This module is to be used in conjunction with the PCM DECODER in a later part of this experiment. As a pair they have a *companding* option. There is compression in the encoder, and expansion in the decoder. In the encoder this means the quantizing levels are closer together for small input amplitudes - that is, in effect, that the input amplitude peaks are compressed during encoding. At the decoder the 'reverse action' is introduced to restore an approximate linear input/output characteristic.

It can be shown that this sort of characteristic offers certain advantages, especially when the message has a high peak-to-average amplitude characteristic, as does speech, and where the signal-to-noise ratio is not high.

T19 *change to 4-bit companding by use of the front panel toggle switch.*

T20 *the TIMS A_4 companding law has already been selected (first Task). Make the necessary measurements to determine the nature of the law.*

Periodic Messages:

T21 *take a periodic message from the SYNC. MESSAGE socket.*

T22 *adjust the oscilloscope to display the message. Record its frequency and shape. Check if these are compatible with the Nyquist criterion; adjust the amplitude if necessary with one of the BUFFER AMPLIFIERS.*
T23 *now look at the PCM DATA output. Synchronize the oscilloscope (as previously) to the frame (FS) signal. Display two or three frames on CH1-A, and the PCM DATA output on CH2-A.*

PCM DECODER:

Clock Synchronization:

A clock synchronization signal will be stolen from the encoder.

Frame Synchronization:

In the PCM DECODER module there is circuitry which automatically identifies the location of each frame in the serial data stream. To do this it collects groups of eight data bits and looks for the repeating pattern of alternate ones and zeros placed there (embedded) by the PCM ENCODER in the LSB position.

PCM Decoding:

The PCM DECODER module is driven by an external clock. This clock signal is synchronized to that of the transmitter. For this experiment a 'stolen' clock will be used.

Upon reception, the PCM DECODER:

1. extracts a frame synchronization signal FS from the data itself (from the embedded alternate ones and zeros in the LSB position), or uses an FS signal stolen from the transmitter .
2. extracts the binary number, which is the coded (and quantized) amplitude of the sample from which it was derived, from the frame.
3. identifies the quantization level which this number represents.
4. generates a voltage proportional to this amplitude level.
5. presents this voltage to the output Vout. The voltage appears at Vout for the duration of the frame under examination.
6. message reconstruction can be achieved, albeit with some distortion, by lowpass filtering. A built-in reconstruction filter is provided in the module.

For the PCM decoding, you will use the PCM decoder module.

Experiment:

A suitable source of PCM signal will be generated using a PCM ENCODER module.

T1 *before plugging in PCM ENCODER module, set the toggles of the on-board SYNC MESSAGE switch SW2. Set the left hand toggle DOWN, and the right hand toggle UP. This selects a 130 Hz sinusoidal message, which will be used later. Now insert the module into the TIMS system.*

T2 *use the 8.333 kHz TTL signal from the MASTER SIGNALS module for the CLK.*

T3 *select, with the front panel toggle switch, the 4-bit LINEAR coding scheme.*

T4 *synchronize the oscilloscope 'externally' to the frame synchronization signal at FS.*

T5 *connect CH1-A of the SCOPE SELECTOR to the PCM OUTPUT of the PCM ENCODER.*

T6 *we would like to recognise the PCM DATA out signal. So choose a 'large' negative DC for the message (from the VARIABLE DC module). From previous work we know the corresponding code word is '0000', so only the embedded alternating '0' and '1' bits (for remote FS) in the LSB position should be seen. Confirm this. They should be 1920 ms apart.*

T7 *vary the DC output and show the appearance of new patterns on CH1-A. When finished, return the DC to its maximum negative value (control fully anti-clockwise).*

The PCM signal is now ready for transmission.

The Receiver (Decoder) :

T8 *use the front panel toggle switch to select the 4-bit LINEAR decoding scheme (to match that of the transmitter)*

T9 *'steal' an 8.333 kHz TTL clock signal from the transmitter and connect it to the CLK input.*

T10 *in the first instance 'steal' the frame synchronization signal FS from the transmitter by connecting it to the frame synchronization input FS of the receiver. At the same time ensure that the FS SELECT toggle switch on the receiver is set to EXT. FS.*

T11 *ensure both channels of the oscilloscope are set to accept DC;*

T12 *connect CH2-A to the sample-and-hold output of the PCM DECODER.*

A DC message:

You are now ready to check the overall transmission from transmitter input to decoder output. The message is a DC signal.

T13 *connect the PCM DATA output signal from the transmitter to the PCM DATA input of the receiver.*

T14 *slowly vary the DC output from the VARIABLE DC module back and forth over its complete range. Observe the behaviour of the two traces. The input to the encoder moves continuously. The output from the decoder moves in discrete steps. These are the 16 amplitude quantizing steps of the PCM ENCODER.*

> You are observing the source of quantizing noise. The output can take up only one of 16 predetermined values.

T15 *draw up a table relating input to output voltages.*

T16 *compare the quantizing levels just measured with those determined in the **PCM encoding**.*

T17 *reset the coding scheme on both modules to 7-bit. Sweep the input DC signal over the complete range as before. Notice the 'granularity' in the output is almost un-noticeable compared with the 4-bit case. There are now 2^7 rather than 2^4 steps over the range.*

T18 *change to a periodic message 3 by connecting the SYNC MESSAGE of the PCM ENCODER, **via** a BUFFER AMPLIFIER, to its input V_{in}. An amplitude of 2 Vpp is suitable. Observe and record the signal at CH2-A.*

Currently the encoding scheme is generating a 4-bit digital word for each sample.

What would be the change to the waveform, now displaying on CH2-A, if, at the encoder, the coding scheme was changed from 4-bit to 7-bit ?

T19 *change the coding scheme from 4-bit to 7-bit. That is, change the front panel toggle switch of **both** the PCM ENCODER **and** the PCM DECODER from 4-bit to 7-bit. Observe, record, and explain the change to the waveform on CH2-A.*

Message Reconstruction:

You can see, qualitatively, that the output is related to the input. The message could probably be recovered from this waveform. But it would be difficult to predict with what accuracy.

Lowpass filtering of the waveform at the output of the decoder will reconstruct the message, although theory shows that it will not be perfect. It will improve with the number of quantizing levels.

If any distortion components are present they would most likely include harmonics of the message. If these are to be measurable (visible on the oscilloscope, in the present case), then they must not be removed by the filter and so give a false indication of performance.

So we could look for harmonics in the output of the filter. But we do not have conveniently available a spectrum analyzer.

An alternative is to use a two-tone test message. Changes to its shape (especially its envelope) are an indication of distortion, and are more easily observed (with an oscilloscope) than when a pure sinewave is used. It will be difficult to make one of these for this experiment, because our messages have been restricted to rather low frequencies, which are outside the range of most TIMS modules.

But there is provided in the PCM ENCODER a message with a shape slightly more complex than a sinewave. It can be selected with the switch SW2 on the encoder circuit board. Set the left hand toggle UP, and the right hand toggle DOWN.

A message reconstruction LPF is installed in the PCM DECODER module.

T21 include the built-in LPF in the output of the PCM DECODER, and observe the reconstructed message. Make comparisons between the 4-bit linear and the 7-bit linear coding schemes.

Companding:

T22 use the front panel toggle switches (on both modules) to select 4-bit companding. Use both 'low' and 'high' level messages into the PCM ENCODER. Check the quantizing characteristic. Record your observations and comment upon them.

Frame Synchronization:

In all of the above work the frame synchronization signal FS has been stolen from the encoder (as has been the clock signal).

The PCM ENCODER has circuitry for doing this automatically. It looks for the alternating '0' and '1' pattern embedded as the LSB of each frame. It is enabled by use of the FS SELECT front panel toggle switch. Currently this is set to EXT FS.

T23 change the FS SELECT switch on the front panel of the PCM DECODER module from EXT FS to EMBED. Notice that frame synchronization is re-established after a 'short time'.

APPENDIX

For a MASTER CLOCK of 8.333 kHz, Table A-1 below gives the frequencies of the synchronized message at the SYNC. MESSAGE output for the setting of the on-board switch SW2.

For other clock frequencies the message frequency can be calculated by using the 'divide by' entry in the Table.

These messages are periodic, but not necessarily sinusoidal in shape. The term 'sinuous' means sine-like.

LH toggle	RH toggle	divide clock by	freq with 8.333kHz clock	approx. ampl. and waveform
UP	UP	32	260.4 Hz	0.2 V_{pp} sine
DOWN	UP	64	130.2 Hz	2.0 V_{pp} sine
UP	DOWN	128	65.1 Hz	4.0 V_{pp} sinuous
DOWN	DOWN	256	32.6 Hz	4.0 V_{pp} sinuous

automatic frame synchronization

The PCM DECODER module has built in circuitry for locating the position of each frame in the serial data stream. The circuitry looks for the embedded and alternating '0' and '1' in the LSB position of each frame.

The search is made by examining a section of data whose length is a multiple of eight bits.

The length of this section can be changed by the on-board switch SW3. Under noisy conditions it is advantageous to use longer lengths.

The switch settings are listed in Table A-1 below.

left toggle	right toggle	groups of eight bits
UP	UP	4
UP	DOWN	8
DOWN	UP	16
DOWN	DOWN	32

Discussion Questions:

1) Define code, code element and code word and describe briefly about binary codes and ternary codes. Which among the two is advantageous for encoding?

2) Describe Line codes and Differential encoding.

3) What are the major sources of noise in a PCM system?