Homework Assignments

Text: Robert K. Dueck: Digital Design with CPLD Applications and VHDL
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Assignment	Due Date
#1: 1-8, 1-10, 1-11, 1-17, 1-19, 1-23, 1-25	9-13
#2: 2-10, 2-21, 2-39, 3-4, 3-16, 3-20, 3-23, 3-35, 3-52	9-20
#3: 6-6. 6-10, 6-22, 6-33, 6-39, 6-48	9-26
#4: You are implementing a DDFS with 20 bit frequency resolution and 12 bit amplitude resolution. a) Compute the memory requirement if you only exploit the quarter wave symmetry of the sine function but apply no further compression techniques. b) Compute the memory requirement if you split the phase argument into3 sections of optimized length. c) What is the maximum amplitude error resulting from you memory compression procedure? d) Write a Matlab script that exactly mimics your DDFS for case a) and b) Calculate the mean square error for each case and create a spectral plot of your synthesized sine function for the following parameters: Sampling Rate: fs=10 MHz Sine frequency 1 100 kHz Sine frequency 2 101 kHz	10-4
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