ELE444 Advanced Electronic Design LAB2

Exercise

Using VHDL, create a seven segment decoder which takes a four bit number and displays it on the seven segment displays. Each segment of the display is considered a separate entity. The pin assignments for each segment and the layout of the displays is given on page 46 of the Trex User Guide. As a first step to creating the decoder, fill in the table below with the correct states of each segment for each character.

Hex	7-Segment bits						
Digits	7	6	5	3	2	1	0
’0’	1	0	0	0	0	0	0
’1’							
’2’							
’3’							
’4’							
’5’							
’6’							
’7’							
’8’							
’9’							
’A’							
’B’							
’C’							
’D’							
’E’							
’F’							

Using the table you filled in, complete the following VHDL code and place the file in a new project. (NOTE: Be sure to set this file as the top level entity of the project if it has a different name than the project name. The filename of this module should be *lab2.vhd since the entity name is* lab2.) To demonstrate the functionality of the circuit, show the TA a simulation in Quartus and realization of the design on the FPGA.

lab2.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity lab2 is

  port (
    ain  : in  std_logic_vector(3 downto 0);
    display : out std_logic_vector(6 downto 0);
selectseg : out std_logic_vector(3 downto 0));
```

```
end lab2;

architecture a of lab2 is
begin  -- a

selectseg <= "1110";

  --           7653210
  display <=  "1000000" when ain = "0000" else  --0
              "1010101" when ain = "0001" else  --1
              "1010101" when ain = "0010" else  --2
              "1010101" when ain = "0011" else  --3
              "1010101" when ain = "0100" else  --4
              "1010101" when ain = "0101" else  --5
              "1010101" when ain = "0110" else  --6
              "1010101" when ain = "0111" else  --7
              "1010101" when ain = "1000" else  --8
              "1010101" when ain = "1001" else  --9
              "1010101" when ain = "1010" else  --A
              "1010101" when ain = "1011" else  --B
              "1010101" when ain = "1100" else  --C
              "1010101" when ain = "1101" else  --D
              "1010101" when ain = "1110" else  --E
              "1010101";                    --F

end a;
```

Assignment

Extending upon the exercise, you should now create a two bit adder. This adder should take the two input digits from the DIP switches - two switches for each digit - on the development board. The result should be displayed on the seven segment output that was created earlier. To implement the adder, use two techniques: the addition operator and logic gates. Demonstrate the operation of this circuit to the TA.

Lastly, extend the 2-bit designs to 8-bits and compare the delay times through a simulation. Does the 8-bit design have four times the delay? Is the delay different between the addition operator and the logic implementation? What type of adder do you think the addition operator utilizes?