Design Project II

Delta-Sigma DAC with High Immunity to Pattern Noise

Introduction

A digital-to-analog converter (ADC) can be thought of as a binary weighted sum realized by an analog summing circuit. Consequently, high-resolution DAC's require very precise weight coefficients. If the resolution exceeds 10 bits, the coefficients cannot be fabricated accurately enough so that a trimming procedure becomes necessary. The coefficient errors can also be tuned in the digital domain by applying an automatic error correction algorithm.

Noise shaping converters provide an alternative approach, which requires neither trimming nor digital error correction [1]. However, effective noise shaping mandates the signal to be sampled significantly above the Nyquist rate. This high sampling rate is characterized by the oversampling ratio (OSR), defined as the ratio of the effective sampling rate divided by the Nyquist rate. Unfortunately, due to the typically very coarse amplitude quantization (frequently to a single bit), noise-shaping converters can suffer from weak nonlinear effects such as limit-cycles, which cause discrete tones (or patterns) in the signal band and thus limit the spurious free dynamic range (SFDR) of the converter.

Project Description

The objective of this project is to build and evaluate a high-resolution digital-to-analog converter, which possesses a dynamic range between 12-15 bits. To achieve such a high resolution without component trimming, the converter will utilize a delta-sigma modulator at its core. Figure 1 shows a typical delta-sigma DAC configuration.

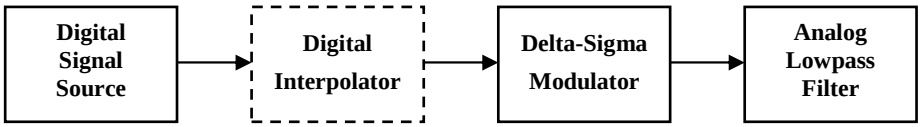

Figure 1: Delta-sigma DAC with digital source and interpolator.

To minimize complexity and cost, we will realize the system without an interpolator. This implies that we utilize a highly oversampled digital signal source (Project I). In the simplest case, we can provide the modulator with a dc input signal. For testing purposes, the analog lowpass will be replaced by a digital memory, i.e., the hard disc on the PC, which stores the modulator output sequence over a sufficiently long time window to yield high-resolution spectral plots (e.g. a window comprising 2^{15} samples).

The delta-sigma modulator architecture to be implemented is the second-order system described in [2]. To detect the potential noise patterns, we will subject the resulting modulator output vector to an autocorrelation function. This computation will be carried out on the host PC.

The DAC implementation and verification system may look as follows:

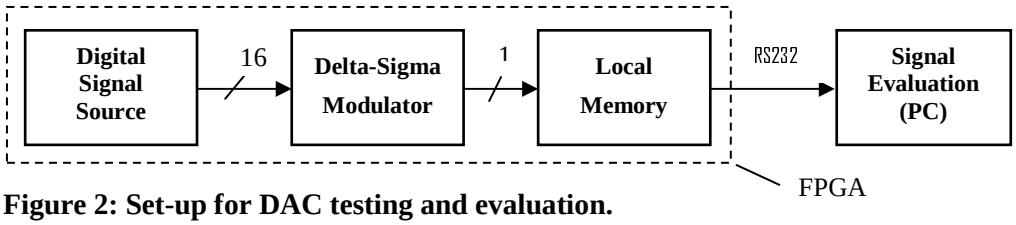

Figure 2: Set-up for DAC testing and evaluation.

Since the modulator is highly oversampled, the data rate of the output signal will be comparatively high (e.g. 6.4-12.8 MHz). Since the communication interface between the FPGA and the PC (RS232) cannot transmit the data in real time, it has to be stored locally. We will first write to a RAM on the FPGA and then send the data to the PC at a later time using a lower transmission rate. In order to effectively evaluate the output spectrum of the modulator via an FFT (Matlab), a minimum vector length of 2^{15} samples will be required.

System Requirements

Delta-Sigma Modulator

- Data path width: 16 bit
- Signal bandwidth: < 50kHz
- Over-sampling ratio (OSR): 64-128
- Resolution: 12-15 bit (SNR: 74-92 dB)
- SFDR > 90 dB

PC Evaluation

1. Pattern noise detection (for dc inputs only)
   - Compute 1000-point autocorrelation function (ACF) for each test run
   - Flag all runs with in-band tones ($f < 1/2\ f_s/OSR$)
2. Frequency spectrum (for arbitrary inputs)
   - Display output power spectrum from dc to ½ f_s
   - Generate spectrum via 2^{15} point FFT (computation is not real-time)

Due Dates for Reports, Demos and Presentations

- Fr 11-02-07 (5pm) Individual progress report # 1
- Fr 11-09-07 (5pm) Individual progress report # 2
- Fr 11-16-07 (5pm) Individual progress report # 3
- Tu 11-27-07 (5pm) Individual progress report # 4
- Tu 12-04-07 Lab Demo # 1
- We 12-05-07 Lab Demo # 2
- Tu 12-04-07 Class Presentation #1
- Th 12-06-07 Class Presentation #2
- **Mo 12-10-07 (5pm)** **Final Project Report** (1 per design team)

References

[1] G. Fischer, and A.J Davis: *Sigma-Delta Modulation*, Encyclopedia of Electrical and Electronics Engineering, John G. Webster, Editor, Wiley & Sons, Inc., vol.19, pp.244-254, 1999 (see Web page ELE444, Lab Handout: **Introduction to Delta-Sigma Modulation)**.

[2] G. Fischer, and D. Hyun: Delta-Sigma Modulator Topologies with high Immunity to Pattern Noise. IEEE Proc. of ISCAS'02, Phoenix, AZ, May 27-29, 2002 (see Web page ELE444, Lab Handout**: Paper on Pattern Noise**).