Home Work Assignment #4

ELE 447

University of Rhode Island, Kingston, RI 02881-0805, U.S.A.

Physical Constants:

$q = 1.6x10^{-19}C$	$\epsilon_o = 8.85x10^{-14}F/cm$
$\epsilon_{ox} = 3.9\epsilon_o = 3.45x10^{-13}F/cm$	$\epsilon_{Si} = 11.7\epsilon_o = 1.04x10^{-12}F/cm$
$n_i = 1.45x10^{10}cm^{-3}$	$\phi_T = 26mV$

Parameters:

$\lambda = 0.3\mu m$	$t_{ox} = 13.9nm$
nMOS & pMOS	
μ_n=$600cm^2/[V-sec]$	μ_p=$300cm^2/[V-sec]$
V_{Tn}=0.75 V	$V_{Tp} = -0.75V$
$C_{j-sw} = 0.34fF/\mu m$	$C_{j-sw} = 0.23fF/\mu m$
$C_{j-A} = 0.41fF/\mu m^2$	$C_{j-A} = 0.72fF/\mu m^2$

---

1) Using your layout of the 4 input nand gate (from lab magic Part A):
   a) Draw the RC equivalent circuit; include ALL source/drain capacitors.
   b) Find the dimensions of each capacitor.
   c) Compute the capacitance of ALL capacitors.
   d) If $R_p = 12k\Omega$ and $R_n = 6k\Omega$, for all transistors, find the rise time (worst case) and the fall time. *Note: for both rise time and fall time measurements, assume that 3 of the inputs are tied to V_{DD} and one input is chaning from HL and LH*

2) Assume that an nMOS transistor has the parameters provided below: $V_{FB} = -0.95V$ $N_A = 3x10^{16}cm^{-3}$ t_{ox}=20nm $V_{T0} = 0.8V$.

   a) Find C_{ox}.
   b) Find ϕ_F.

[1] Tel: (401) 874-5482; fax: (401) 782-6422; e-mail: davis@ele.uri.edu

c) Find Find the body factor, γ.
d) Find $\frac{Q_{B0}}{C_{ox}}$ & Q_{B0}.
e) Find the *native* threshold voltage, $V_{Tnative}$.
f) Find the implant charge, Q_I and the implant surface density N_{im} (Hint: $Q_I = qN_{im}$).
g) Compute the change in the threshold voltage ΔV_T, the threshold voltage V_T, and $V_{DD} - V_T$ for $V_{SB} = 0$, 1, 2, 3, 4 & 5 Volts. (assume $V_{DD} = 5V$).

3) The nMOS transistoris configured as shown in figure 1. The initial value of node $V_x = 0V$ and node $V_G = 0V$. Then, $V_G = V_{DD}$. Answer the following questions:

a) Derrive an expression which relates V_x to V_{TH_p} (assume only strong inversion; in other words if $V_{GS} < V_T$ then the transistor will be OFF).
b) Use the previous part of this problem to find the highest value of V_x. (Hint: you have already computed this answer in the previous problem).
c) Try the same problem with a pMOS transistor; replace the voltage source with a short to ground and assume that $V_x = V_{DD}$; V_G is switched from High to Low.

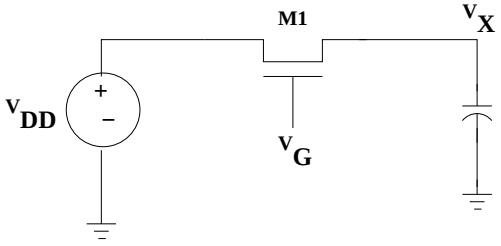

Figure 1. Schematic for problem #3.

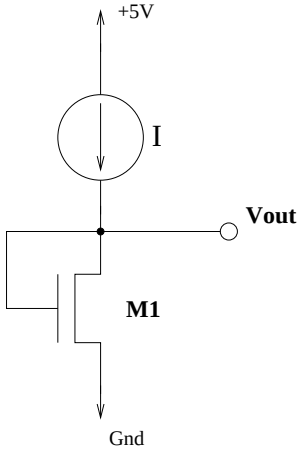

Figure 2. Schematic for problem #4.

4) For the transistor shown in figure 2 the following information is given: $(W/L) = (6\mu m/2\mu m)$;(I = 420 μA).

a) Show that M1 will always remain in saturation (assuming it is "on").
b) Compute β_n.
c) Compute I_{DS}.
d) Write the equations (and only those) needed to find the value of V_o.
e) Compute V_o.
f) What happens to V_o if I_{DS} is reduced by 50 % ?? Repeat I_{DS} if doubles.

5) The following information is given for the inverter shown in figure 3: V_b = Gnd, $(W/L)_n$=($8\mu m/2\mu m$) & $(W/L)_p$=($4\mu m/2\mu m$)

   a) Compute β_n & β_p; Compute $\left(\frac{\beta_n}{\beta_p}\right)$.
   b) For what values of V_b will M1 be ON ?
   c) Does this inverter pull up to V_{DD} ? Does it pull down to Gnd ?
   d) Assuming that M1 goes into saturation when $V_{out} = V_{OL}$, find V_{OH} & V_{OL} ?
   e) Sketch the DC transfer characteristic, e.g., V_{out} vs. V_{in}. Find the exact values where each transistor's region of operation changes; label these values on the plot.
   f) Perform DC analysis in HSPICE using the level 1 model parameters provided; does the HSPICE plot agree with your sketch ?

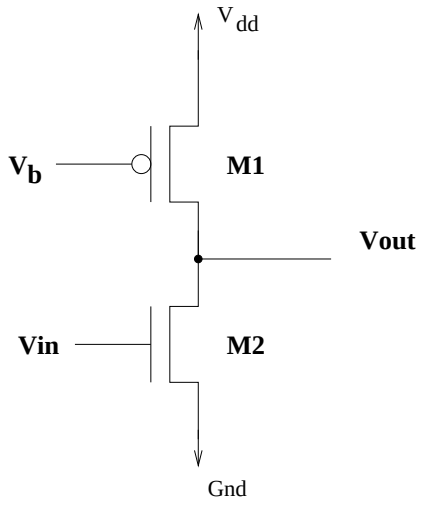

Figure 3. Schematic for problem #2, 3.

6) The following information is given for the inverter shown in figure 3: V_b = 2.5 V, $(W/L)_n$=($4\mu m/2\mu m$) & $(W/L)_p$=($8\mu m/2\mu m$)

   a) Compute β_n & β_p; Compute $\left(\frac{\beta_n}{\beta_p}\right)$.
   b) Does this inverter pull up to V_{DD} ? Does it pull down to Gnd ?
   c) Sketch the DC transfer characteristic, e.g., V_{out} vs. V_{in}. Find the exact values where each transistor's region of operation changes; label these values on the plot.
   d) Perform DC analysis in HSPICE using the level 1 model parameters provided; does the HSPICE plot agree with your sketch ?