Home Work Assignment #2

Due 21 September 2011

ELE 447

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Physical Constants:

$q = 1.6x10^{-19}C$ $\epsilon_o = 8.85x10^{-14}F/cm$

$\epsilon_{ox} = 3.9\epsilon_o = 3.45x10^{-13}F/cm$ $\epsilon_{Si} = 11.7\epsilon_o = 1.04x10^{-12}F/cm$

Process Parameters:

$\lambda = 0.3\mu m$ $t_{ox} = 13.9nm$

nMOS & pMOS

$C_{j-sw} = 0.34fF/\mu m$ $C_{j-sw} = 0.23fF/\mu m$

$C_{j-A} = 0.41fF/\mu m^2$ $C_{j-A} = 0.72fF/\mu m^2$

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1) Read over the section in the lab manual, chapter 2, section 2.2, describing the ring oscillator operation. Consider this; an 11 stage ring oscillator can be realized by connecting 11 identical inverters in a series ring. This means that the output of the first inverter is connected to the input of the second inverter, ... and the output of the 11^{th} inverter is connected to the input of the first inverter. The expression that relates the frequency of the ring oscillator to the propagation delay in each individual inverter is given by:

$$f = \frac{1}{T} = \frac{1}{2n\tau_d} \tag{1}$$

where f is the frequency of the ring oscillator and τ_d is the propagation delay of a single inverter. Note that the propagation delay is the average of the rising and falling delay (e.g. $\tau_d = \tau_{dp} = \frac{(\tau_{dr}+\tau_{df})}{2}$). I have provided a spice netlist to simulate the ring oscillator. The new netlist incorporates many of the spice features that you will need for the Hspice B laboratory exercises.

a) Download the spice netlist (ring11F2011V1.sp). Examine the inverter stage; notice that $C_L = 232fF$. Also notice that this netlist simulates

an 11 stage ring oscillator and it also measures the delay of the individual inverter used in the ring oscillator.

b) Compute the gate capacitances using the values for C_{OX} (and t_{OX}) from lab 1. Use the gate geometries (e.g. W and L (scaled by $0.3\mu m$) specified for the inverter in ring11F2011V1.sp.

c) Run the ring oscillator netlist (hspice ring11F2011V1.sp > prob1c.lis); scroll backwards up the screen and you will see the outputs of measure statements. Pay close attention to the following delays: tdf, tdr, $tdlyf$, $tdlyr$ and $freq1$. These outputs are taken from automatic measurements. tdf and tdr are the measurements of the individual inverter for the falling and rising delay, respectively. $tdlyf$ and $tdlyr$ are falling and rising delay measurements taken from one of the inverters placed inside the ring oscillator. $freq1$ is the HSpice measurement of the ring oscillator frequency.

d) Use the expression in equation (1) to find τ_{dp} from $freq1$. Is this reasonably close to the delay of the individual inverter (examine the values of (tdf, tdr and compare to $tdlyf$ and $tdlyr$).

e) Edit the netlist file, ring11F2011V1.sp. Change the load capacitance to $C_L = 10f$. Repeat your analysis (hspice ring11F2011V1.sp > prob1e.lis);.

f) Is the inverter delay predicted by equation (1) still close to the measured delay of an individual inverter ?

2) Download the spice netlist ring11F2011V2.sp. Simulate this ring oscillator in hspice (hspice ring11F2011V2.sp > prob2.lis); record the values for $freq1$, tdf, tdr, $tdlyf$, and $tdlyr$. These values represent the same measures, e.g. ring oscillator frequency, the falling and rising delay of an individual inverter and finally, the falling and rising delay of an inverter placed inside the ring oscillator. Compare these measurements to those of the previous problem. Also, determine if equation (1) accurately predicts a propagation delay which is close to the measured propagation delay of the individual inverter.

3) Create a 31 stage ring oscillator. Modify the spice netlists, ring11F2011V1.sp and ring11F2011V2.sp (and change the file names to something like ... ring31V1.sp, ring31V2.sp). Run each netlist in hspice to verify they will run.

4) Text Book Problems (note: change the $f =$ to $g =$):

a) 1.1

b) 1.2

5) Find β_n for $\mu_n = 500\ \frac{cm^2}{[V-s]}$ for $(W/L)_n = 1$. Find the exact units for β_n. Can you show that the units of β_n are equal to $[\frac{\mu A}{V^2}]$??

6) The rise time for a logic gate is often defined as the time it will take the output voltage, V_{out}, to rise from $10\%V_{DD}$ to $90\%V_{DD}$ (where V_{DD}, the supply rail, is the maximum output voltage level). The fall time of a logic gate is defined as the time it will take the output voltage, V_{out}, to fall from $90\%V_{DD}$ to $10\%V_{DD}$.

   a) Using a simple "pull-up" RC model, show that:
   $T_{rise} = 2.2RC_L$.

   b) Using a simple "pull down" RC model, show that:
   $T_{fall} = 2.2RC_L$. where R is the switch resistance and C_L represents the capacitive load.

   c) Suppose that V_{dd} changes from 5 Volts to 3.3 Volts. How do the expressions for rise time and fall time change ?

   d) Suppose the rise time definition is changed to the time difference between the time V_{out} rises from 0 Volts to $70\%V_{DD}$. Also assume that the fall time definition is changed to match the rise time definition (e.g. V_{out} falls from $70\%V_{DD}$ to 0 Volts). How do the expressions for rise and fall time change ?

   e) Repeat part (d) for a maximum level of 3.3 volts.