University of Rhode Island Department of Electrical and Computer Engineering
ELE 447: Digital Integrated Circuit Design I

Lab 5 Report Format (including some of the previous labs)

1 Report Format

1. Show the simulation results of Inverter extracted from MAGIC (Use 0.1pF load cap) using IRSIM. compare the results with HSPICE and comment on the results (such as propogation delays)
2. Show the simulation results of NAND/NOR gates using IRSIM, you can use the library cells. (Use 0.1pF load cap). compare the results with HSPICE and comment on the results (such as propogation delays)
3. Show the Results/plots of the Ring Oscillator (for a 7 or 9 inverter case). Show the simulation results using HSPICE and IRSIM. Comment on the differences.
4. Show the magic layout and simulation results of Xor Gate (using CMOS Transmission Gates, schematic shown in lab4 handout)
5. Show your 2:1 Mux magic layout. And the magic layouts of 4:1, 8:1, 16:1 Muxes using 2:1 Mux as the building block.
6. Show and comment on the simulation simulation results (if you havent done yet).
7. Work on the static latch. Show the magic layout and simulation results of a static D-latch, static D-flip flop and T-flip flops. Try to simulate them using HSPICE and IRSIM.
8. Try to look into counters and the modulo-10 counters.

2 Grading format

The lab will be graded for a total of 10 points.

1. 3.5 points for MAGIC Layouts.
2. 3.5 points for showing the results/HSPICE simulations.
3. 3 points for justification of the results.

3 Feedback

I would appreciate if you take few minutes to write any general comments about the lab. (for example: what did you like about the lab and what you didnt, so forth).

You can work in groups but everybody should submit an individual report. The lab report is due in a week.

If you have any other questions, you can send me an email at vijay@ele.uri.edu or stop by the ESP lab Kelly 201.