ELE447 Lab 3: Ring Oscillators and Sub-circuits

By cascading several inverting logic gates (e.g. inverters) and connecting the last output to the first input, a loop is formed. Based on the number of gates in the loop, two outcomes are possible:

1) If the number of inverting gates is even, the last output equals the first input.
2) If the number of inverting gates is odd, the last output is the complement of the first input.

Figure 1 depicts an example of case 1, where 2 inverters are connected in a loop. If V1 represents a logic 0, its output, V2, becomes high, which in turn forces the output of the second inverter, V1, to a low logic state. Since the two inverters in this configuration preserve their outputs, the loop is stable. This circuit is called a latch.

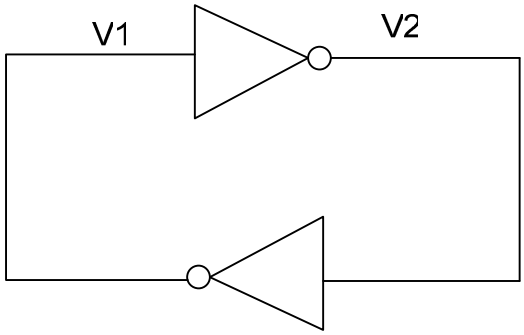

Figure1. A simple latch

Figure 2 depicts an example of case 2 above with three inverters connected in a loop. Let us assume V1 represents a logic 0. This signal propagates through the loop and will eventually change the output of the third inverter from a logic 0 to a logic 1. This change of the input state will again propagate through the loop and eventually flip the input state again. As a matter of fact, all 3 inverter outputs in this configuration will change their state at the same toggling rate. This circuit is called a ring oscillator.

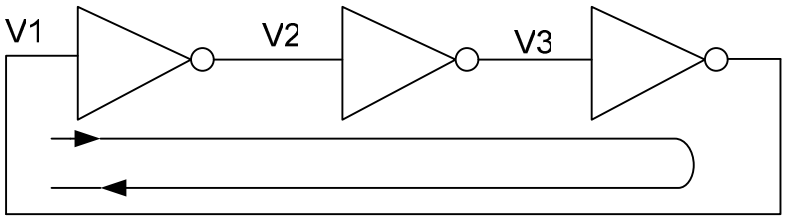

Figure2. A simple ring oscillator consisting of three inverters

The analysis of ring oscillator is quite simple. Suppose there are N inverters in the loop and the input of first inverter, V1, is a logic 0. If the propagation delay of each inverter is τ_{pd}, where $\tau_{pd} = \frac{1}{2}(t_r + t_f)$, the total loop delay will be N τ_{pd}. V1 therefore remains

either high or low for N τ_{pd} seconds. The period of the oscillation thus becomes $T_{osc}=2N\tau_{pd}$. This yields an oscillation frequency of:

$$f_{osc} = \frac{1}{2N\tau_{pd}} \qquad (1)$$

Equation 1 is a simple relationship between the oscillation frequency, the number of inverters and the (average) propagation delay of each logic cell.
The propagation delay of each inverter is a function of the time constant experienced by the driving gate as illustrated in Figure 3. The delay time constant is the product of the on resistance of the driving gate and the (parasitic) output capacitance Cp. We have previously learned that the equivalent gate resistance and the output capacitance are both related to the inverter transistor dimension. We can therefore control the oscillation frequency by controlling the transistor geometry. Obviously, a smaller geometry will increase the frequency of oscillation.

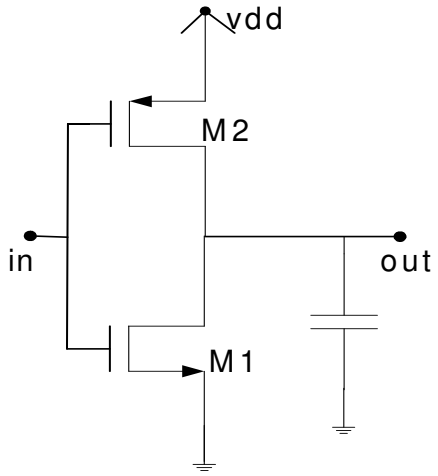

Figure3. An inverter cell

Propagation delay measurement of different gates

A ring oscillator circuit can be used as a tool to measure the propagation delay of a simple inverter or other simple inverting cells such as NAND and NOR gates.
A ring oscillator represents a preferred method for measuring the propagation delay of a logic gate (cf. eq.1), since it measures the cumulative rise and fall times of N gates under realistic operating conditions. Because any measurement error is divided by N, the ring oscillator also provides a very accurate measurement of the propagation delay.

Let us begin by considering a ring oscillator circuit consisting of 10 inverters and one NOR gate connected in a loop. We use this circuit to measure the propagation delay of a single inverter driving another identical gate. Figure 4 depicts such a ring of gates. We use the NOR gate to set the initial state of each node. To accomplish this, we apply a positive pulse to the *free* input of the NOR gate. This keeps the NOR output low, independent of the state of the other input. The width of the applied pulse must be long

enough to initialize all gates. Conversely, when we set the pulse low, the NOR gate acts like a regular inverter.
Simulate the circuit with HSPICE and measure the frequency of oscillation and compute the average inverter propagation delay. Run your simulations for the 2 supply voltages of 5V and 3.3V. Explain the results.

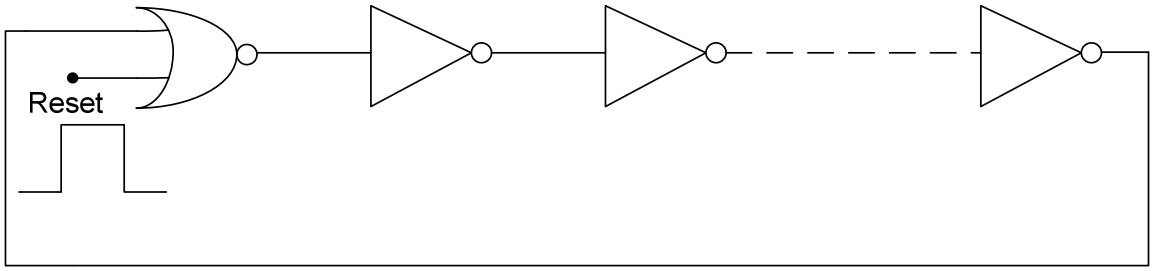

Figure4. A ring oscillator compromising 10 inverters and one nor gate to set initial states of nodes

The same procedure can be applied for measuring the propagation delay of a 2-input NAND gate as shown in Figure 5. To do so, we switch the 2 inputs of each NAND gate in parallel, while the NOR gate acts again a reset element.
Simulate this circuit with HSpice and determine the oscillation frequency and the average propagation delay of a 2-input NAND gate. Compare the new results with the corresponding values obtain from the previous simulations and explain the differences.
Finally, apply the same procedure to a loop of 11 NOR gates.

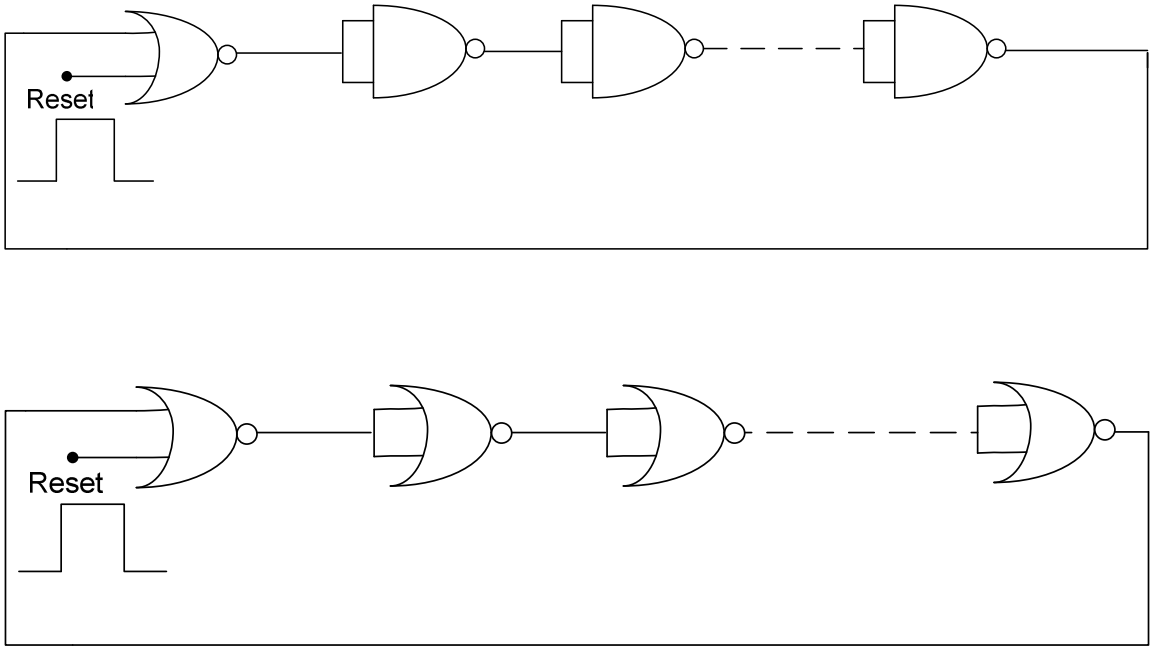

Figure5. Ring Oscillators incorporating NAND and nor gates.

SUB-Circuits in HSPICE

If the same circuit is a repetitively used in a certain netlist, its is practical to define this circuit as a **sub-circuit**. Defining a sub-circuit allows you to avoid duplicating and writing unnecessary long netlists. For example, a ring oscillator comprising 31 identical gates can be described by a single sub-circuit netlist and 31 sub-circuit calls.

.SUBCKT subnam n1 < n2 n3 …>

The netlist of sub-circuit

.ends

The definition of an inverter as a sub-circuit for ring oscillator is given below.

```
.subckt  inva  out in vdd  vss
M1  out   in  vdd   vdd  pfet   w=10  l=2
M2  out   in   vss    vss   nfet   w=4    l=2
.ends
```

The Subcircuit Call Statement:
To use a defined sub-circuit on your netlist, you can call that sub-circuit using the syntax below:

Xyyy n1 <n2 n3 …> subnam
Like:
X1 1 2 dd gnd
This implies an inverter with output node 1 and input node 1.