Master of Memory

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The people at Innovative Silicon, a company in Switzerland, have developed a new microprocessor technology that has been described as the densest and cheapest embedded memory technology in the world.

This technology is called the Z-RAM, which stands for zero-capacitor dynamic random access memory. This technology does not require any new materials or extra processing steps in the fabrication process. Each memory is just a single transistor. Current on-chip memory devices typically use six transistors per memory cell. Basically, this means as much as five megabytes of Z-RAM into the space occupied per single megabyte of conventional embedded memory. This way, manufacturers could greatly increase the amount of memory able to fit on each chip or they could significantly reduce the size of the chip used. Either way, the technology is monumental.

To make this Z-RAM work, the Innovative Silicon Company found a way to temporarily store a bit as charge inside the body of a transistor made on a semi-conductor wafer. This effect causes capacitance to form between the transistor and the underlying insulating substrate, and was a problem that needed to be solved in conventional designs. Consisting of only one part instead of two, Z-RAM offers twice the density of DRAM and five-times of SRAM.

The small size of Z-RAM actually makes its processing faster. Although Z-RAM's individual cells are not as fast as SRAM, the lack of long lines allows a similar amount of cache to be run at roughly the same speeds by avoiding this delay while taking up less space. The response of Z-RAM is as low as 3 nanoseconds have been observed.

Z-RAM is a technology that encompasses two great industry imperatives: ever more on-chip memory and transistors that operate faster and consume less power. For the makers of microprocessors, gains in speed and efficiency are coming from the use of silicon-on-insulator (SOI) wafers. SOI wafers differ from an ordinary silicon wafer in that it has a very thin layer of insulating silicon dioxide buried a few hundred nanometers or less below the surface. That layer of insulation cuts the transistor off from the vast bulk of the wafer. This limits the amount of charge that transistor must move in order to switch on or off. This causes an increase of speed of about 30 percent.

All of these advancements come at a cost of about $275 for a 200-millimeter SOI wafer. However, the cost can be made up with the technology of storing more memory on each SOI wafer.

As the Z-RAM transistor shrinks, it stores less charge, but the effect of that charge on the current through the transistor only grows stronger. Since it's the current, not the charge, that reads the bit, Z-RAM should work even with much smaller transistors.

The Z-RAM technology can save 10%-40% in chip costs and it can embed over four times the memory at the same cost yet requires no additional manufacturing costs and no special materials. Z-RAM also uses a standard SOI logic process which is useful for all the products that currently run on this type of logic.

Z-RAM also proves to be extremely flexible and provides excellent results in anything from ultra-low power memories for cell phones to high-performance memories for microprocessors.

Works Cited

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