Research at Intel
Microarchitecture

Intel research and development is a decentralized worldwide network of researchers, scientists and engineers who are pioneering technology innovation and catalyzing cooperation within the computing and communications industry. With a network of over 7000 technology professionals, Intel can focus on developing breakthroughs in a variety of areas, including silicon technology and manufacturing, microarchitecture and circuits, computing platforms, communications and networking, and software technology. For more than 30 years, the company's research and development activities have continually expanded the possibilities for enhancing peoples lives and work through computing and communications.

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In the last decade, designers relied on instruction level parallelism to improve processor performance. Today, as transistor density continues to grow at the pace predicted by Moore's Law, ILP techniques are yielding diminishing returns. That's just one of the challenges microarchitecture researchers face as advanced technology solutions create new and complex problems. To meet these challenges, Intel is building a world-class team of microarchitecture researchers.

Building a World-Class Research Team

Intel's deep knowledge and experience in advancing microarchitecture design have enabled us to lead the industry for more three decades. By attracting some of the best microarchitecture researchers in the world to Intel, we are helping to ensure our leadership position for decades to come. In these pages, we will highlight Intel's microarchitecture research agenda, tell you about our global, collaborative approach, and introduce you to some members of our research team.

Research on a Global Scale

Intel research centers are located throughout the world. Microarchitecture research is conducted at four centers in the United States as well as a facility in Israel and, since February 2002, one in Barcelona. With the launch of Intel Labs Barcelona (ILB), we reaffirmed our commitment to locating new centers in close proximity to top researchers, anywhere in the world, whose specific expertise will strengthen our research team. ILB is located nearby a university with a group of world-renowned microarchitecture researchers who now conduct joint investigations with Intel.

Shaping the Future

One of Intel's strengths is translating groundbreaking research into innovative technology products. Our microarchitecture researchers have the satisfaction of knowing the work they do today will influence the products and platforms of tomorrow. Their research is helping to shape the future of computing and communications.

As technology advancements render old design paradigms obsolete, our research team is pursuing exciting new design directions, from thread level parallelism to "power-aware" architectures. There is no better time to be a microarchitecture researcher. And no better place than Intel.

Research Agenda

Intel's microarchitecture research agenda focuses on two key areas — performance and power — and the tools and methods required to support these avenues of research. Our researchers are pursuing a range of investigations, all focused on developing world-class microarchitectures for established and emerging platforms. The following pages provide an overview of research underway.

"We take new Ph.D.s, armed with creativity and the latest innovative ideas, and pair them with veteran microarchitects who know what it takes to build a successful product. Both sides learn and grow from the experience and produce the best research results."

John Shen
Director, Microarchitecture Research
California, USA

Collaboration on a Global Scale

At Intel, we believe that close collaboration among microarchitecture researchers expands their skills and knowledge and advances the state of the art in microarchitecture design. With that in mind, we take several steps to encourage collaboration in many forms.

Pairing novices and veterans

One step is to pair new recruits, armed with creativity and the latest innovative ideas, with veteran microarchitecture researchers who have practical experience in developing successful products. Pairing a novice with an experienced team member enriches both, and it generates higher quality research results.

Collaborations between locations

Our researchers also collaborate across geographic locations, communicating frequently and engaging regularly in joint investigations. This close collaboration among Intel researchers worldwide ensures that the latest ideas are quickly disseminated throughout the company and that our collective knowledge base continually advances.

Working with product groups

Many of our microarchitecture researchers work closely with product development groups, as research insights evolve into new product designs. Through these working relationships, researchers gain a better understanding of the real-world problems and constraints that developers face, and these insights inform future research. Over time, such liaisons have enabled Intel to maintain an outstanding track record of translating research into innovative technology products.

Linking to the global research community

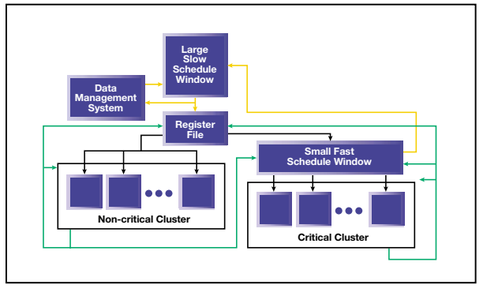
In addition to collaborating internally, Intel's microarchitecture researchers maintain close ties to the global research community. Our researchers are active in professional conferences and symposia, collaborate extensively with academic researchers, and have an impressive track record of publications in leading technical journals. This active participation in the global research community, along with Intel's support of academic research via grants and internships, enables us to stay in the forefront of microarchitecture research.

Performance

Intel has consistently delivered on Moore's Law for three decades, doubling the number of transistors per square inch on integrated circuits every two year The goal of our performance-related research is to continue translating these additional transistors into useful performance improvements.

"Microarchitecture research at Intel gives us the opportunity to simultaneously appreciate and address the issues and constraints of current product development, and to contribute results with a more general and longer-term perspective."

Joel Emer
Intel Fellow
Director, Microarchitecture Research
Massachusetts, USA



Parallelism

To improve performance, we are pursuing parallelism at three levels: instruction, thread, and memory. We continue to refine the ILP techniques of the last decade, but as the returns on this approach diminish, we are exploring thread level parallelism (TLP) and memory level parallelism (MLP) to achieve additional performance improvements.

"As we reach the limits of ILP, we're looking for new ways to extract parallelism at the thread level. Through our research, we are now using speculative TLP techniques to parallelize applications that in the past we thought it would be impossible to parallelize."

Antonio Gonzalez
Professor, Computer Architecture
Director, Microarchitecture Research
Universitat Politècnica de Catalunya, Barcelona, Spain

Thread Level Parallelism

We are pursuing a variety of multithreading techniques to improve performance by executing multiple threads simultaneously within one processor or multiple processor cores. One approach involves identifying predictable threads that can be executed in parallel, by analyzing program features and predicting future control flows and data values. This approach is enabling us to parallelize applications that in the past were thought to be impossible to parallelize. We are designing both the microarchitecture and the compiler techniques to support this new execution model.

Memory Level Parallelism

The memory hierarchy has become a major performance bottleneck, as the speed differential between processor and memory continues to grow at a rapid rate. We are exploring memory level parallelism to address this memory latency problem. By applying MLP techniques to perform multiple memory operations simultaneously, we can reduce average latency. One approach we're trying entails the use of helper threads to prefetch data and instructions from lower-level slow memory into higher-level fast caches.

"Memory has become a key performance bottleneck. We are using helper threads to assist us in tackling the memory latency problem."

Hong Wang
Principal Researcher
Microarchitecture Research
California, USA

Software-hardware synergy

Historically, software was used to optimize code at compile time and hardware was used to perform optimization at run time. Now there's a blurring of boundaries. Today we are using both hardware and software at compile time and run time to generate optimal performance. Our researchers are searching for new ways to achieve even greater synergy between hardware and software by appropriately redefining the dynamic-static interface.

"The lines between hardware and software are blurring, as are the lines between run-time and compile-time techniques. We're looking for more ways to create synergy between static and dynamic optimizations, and redefining the hardware and software interface."

Geoff Lowney
Intel Fellow
Director, Microarchitecture Research
Massachusetts, USA

Microarchitecture for enterprise servers

Intel's entry into the market for enterprise servers is generating new opportunities and challenges for microarchitecture researchers. As advances in technology have enabled us to put more and more functionality on a chip, the historical boundary between macroarchitecture (or system architecture) and microarchitecture has blurred. As a result, microarchitecture researchers now find themselves essentially designing system architectures on a chip, and facing new challenges traditionally associated with macroarchitecture research. For example, traditional multiprocessor and interprocessor network communication and synchronization are becoming issues that microarchitects must deal with in the design of a single chip.

"During the past decade, we have become very good at simulating IPC for arbitrary microarchitectures. More recently, we have started to measure power on the microarchitectural level. Over the next ten years, we must learn how to quantify the effects of microarchitecture on a processor's frequency, die area, and design time."

Ed Grochowski
Principal Researcher
Microarchitecture Research
California, USA

Power

Power consumption and heat dissipation are serious limiting factors in microprocessor performance and present complex challenges for microarchitecture researchers. Our research objective is to generate continued performance improvements by managing power and thermal issues effectively.

"We must resolve power and thermal issues if we are to maintain increasing processor speeds. Our research into power aware architecture is vital to keeping us on the curve of Moore's Law."

Ronny Ronen
Principal Researcher
Director, Microarchitecture Research
Haifa, Israel

Power-aware architecture

We are exploring new architectures that are conscious of power and thermal issues and able to manage them dynamically while running applications. Some approaches we are investigating include multi-core and clustered microarchitectures as well as new, revolutionary architectural and microarchitectural paradigms.

"Developing new tools is an important part of our research work. Our ability to model power and thermal characteristics before we build a system is helping us to choose the right trade-offs when designing new microarchitectures."

Aviad Cohen
Senior Researcher
Microarchitecture Research
Haifa, Israel

Multi-core and clustered microarchitectures

We are examining the concepts of multi-core and clustered microarchitectures to increase overall performance while managing power more effectively. Our unique approach focuses on CPU cores and clusters that perform optimized load balancing among cores and clusters through a combination of software and hardware mechanisms that dynamically examine the load, priority, thermals and criticality of processes. Our goal is to reduce overall power requirements while increasing performance.

Power Optimized Microarchitecture

We are researching new microarchitecture innovations and instruction set extensions that will provide more performance at lower power by producing more results with less work. Architecturally, we strive to achieve this by squeezing more useful activity into each machine instruction, thus significantly reducing overhead. At the microarchitecture level, we attempt to eliminate redundancy by identifying frequent instruction sequences extensively optimizing them, and storing and reusing them later.

"At Intel research we don't just strive for bigger, better, faster. We also seek lower power and less expensive, more reliable processors."

Srilatha Manne
Senior Researcher
Microarchitecture Research
Massachusetts, USA

"Intel is attracting some of the top microarchitecture researchers in the world. The addition of UPC adds an exciting new dimension to our internal research community."

Roger Espasa
Professor, Computer Science
Director, Microarchitecture Research
Universitat Politècnica de Catalunya, Barcelona, Spain

Power cont'd

Managing Communication Delays

As microprocessors get faster and more transistors are put on a chip, it takes relatively longer for signals to propagate. This can cause communication delays that inhibit performance. To address this problem, researchers must develop techniques to identify critical data and design microarchitectures that will route that data along the shortest paths. Techniques to expose and exploit communication locality are going to be critical for future microprocessors. Clustered microarchitectures is one of the approaches we are investigating to deal with this issue.

"Our advanced development work focuses on the demanding applications of the future."

Antonio Juan
Professor, Computer Science
Director, Microarchitecture Research
Universitat Politècnica de Catalunya, Barcelona, Spain

"During the last decades, processors tended to do more bookkeeping and less real work. We are going to change that. We have to design more efficient processors that do more useful work per instruction."

Gad Sheaffer
Senior Researcher
Microarchitecture Research
Haifa, Israel

Intel Labs Barcelona

With the launch of Intel Labs Barcelona (ILB) in February 2002, Intel established its first microprocessor R&D facility in Europe. In this new facility, Intel is conducting joint microprocessor research and development with the Universitat Politècnica de Catalunya (UPC).

World-renowned researchers

UPC was chosen for its world-renowned team of computer architecture researchers. With the establishment of ILB, Intel is laying the groundwork for long-term collaborations with UPC.

A unique arrangement

ILB is operated for Intel by UPC. Many researchers at the center, located on the UPC campus, will remain UPC employees and will maintain their academic status. This unique arrangement will enable ILB to work with some of the best microprocessor researchers in Europe without separating them from the European academic community.

Enhancing Intel's research capabilities

ILB will enhance Intel's industry-leading microarchitecture and compiler research capabilities in key technology areas. These include new microarchitectures and compiler techniques for power-aware processors and high-performance processors that exploit speculative thread level parallelism and data parallelism.

Tools and Methods

In addition to conducting investigations into performance and power, we develop tools and methods to support research in these areas. Such tools and methods are an important ongoing aspect of our microarchitecture research. We continuously strive to increase their accuracy and flexibility, to enable our researchers to continue working at the leading edge of the industry. A few examples of tools and methods we have developed and are refining:

"Using multiple cores gives us much more flexibility in managing power consumption and heat dissipation while achieving higher performance."

Doron Orenstein
Doron Orenstein
Principal Researcher
Microarchitecture Research
Haifa, Israel

"To continue extending Moore's law, we will have to explore entirely new microarchitectural techniques. The challenges are daunting but exciting."

Jared Stark
Senior Researcher
Microarchitecture Research
Oregon, USA

- Methods of modeling multithreaded and multiprocessor workloads more accurately.
- Visualization tools that graphically depict the behavior of a simulated microarchitecture, to generate new design insights not easily gleaned from numeric models.
- Modular simulation tools to evaluate power, performance, integrity and functionality — the four critical processor characteristics — before a machine is built. Among these tools are a simulator used early in the design cycle, to test microarchitectural structures and determine tradeoffs among alternative structures, and a tool used later in the cycle, to explore design tradeoffs. These highly modular simulation tools enable us to explore structural and design alternatives easily, using any configuration of components.

"Current projections show that transient faults in processors due to neutron particle strikes are increasing at an alarming rate, thereby reducing processor reliability. We are working on measuring, detecting, and protecting processors from such failures."

Shubhendu Mukherjee
Senior Researcher
Microarchitecture Research
Massachusetts, USA

Learn More About Our Team

We are entering a new era of microarchitecture design, as advances in semiconductor technology create boundless opportunity for using transistors in new ways. For researchers, the challenges-and the potential to make an impact-are enormous. More than ever before, microarchitecture researchers are helping to shape the future of computing and communications. Intel offers career opportunities in microarchitecture research to qualified Ph.D.s and Ph.D. candidates. To learn more about our research team, to read our publications, and to view profiles of team members, visit www.intel.com/research. For information about current opportunities, visit www.intel.com/jobs.