

# QING (KEN) YANG 杨庆

Tel: (401) 874-5880

Fax: (401) 782-6422

E-mail: qyang@ele.uri.edu

<http://www.ele.uri.edu/~qyang>

## TITLE

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**Distinguished Engineering Professor,**

Department of Electrical, Computer, and Biomedical Engineering, University of Rhode Island

## EXPERIENCES

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1997–Present *Professor* Dept. of ECE, University of Rhode Island Kingston, RI

1993–1997 *Associate Professor* Dept. of ECE, University of Rhode Island Kingston, RI

1988–1993 *Assistant Professor* Dept. of ECE, University of Rhode Island Kingston, RI

## EDUCATION

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**Ph.D.** with honor, Computer Engineering, The Center for Advanced Computer Studies, University of Louisiana, Lafayette, USA, June 1988.

Dissertation Title: Analysis of Cache-based Multiple-bus Multiprocessors.

**M.A.Sc.**, Dept. of Elec. Engin., University of Toronto, Canada, Nov. 1985.

Thesis Title: Communication Performance in Multiple-bus Systems.

**B.Sc.**, Dept. of Computer Science, Huazhong University of Science and Technology, People's Republic of China, Feb. 1982. Ranked First in the graduating class.

## AWARDS AND HONORS

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- **IEEE Fellow** for contributions to computer memory and storage systems.
- EMC Endowed Visiting Chair Professor, Tsinghua University, China, 2008.
- Outstanding Intellectual Property Award, University of Rhode Island. 2008
- Aurelio Lucci Faculty Excellence Award for Outstanding Entrepreneurship, URI, 2007;
- Outstanding Intellectual Property Award, University of Rhode Island. 2007
- Outstanding Intellectual Property Award, University of Rhode Island. 2005
- Albert E. Carlotti Faculty Excellence Award, College of Engineering, URI, 2005.
- “Yellow Crane Friendship Award” for Outstanding work on scholar activities and technology transfers, Wuhan, China, Sept. 2002.
- Cover story on International Talent Magazine June 2002.
- Keynote Speech at 2002 Shen Zhen HI-TECH Fair, Oct. 2002.
- On the National News of China, People's Daily (overseas edition), 2002
- Outstanding Intellectual Property Award, University of Rhode Island. 2001
- 10 Best HUST alumni overseas, 2000
- “A novel cache on data storage”, A news article on Horizons, Spring 1999.

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- *Distinguished Engineering Professor*, College of Engineering, URI, since Jan. 1998.
  - Listed in “Who Is Who Among Asian-Americans,” 1993 and “Who Is Who in America,” 1994.
  - Aurelio Lucci Faculty Excellence Award, for excellence in teaching, research and services, URI,
  - Outstanding Young Man of America, 1992
  - NSF (National Science Foundation) Research Initiation Award, RIA Award 1989

## **US PATENTS AND TECHNOLOGY TRANSFERS**

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Note: 7 of the following patents have resulted in license income to URI for over hundreds of thousands of dollars.

1. “Prime-Mapped Cache---A new cache memory system for vector processings,” US Patent No. 5,379,39.
2. “Disk Caching Disk---A new architecture for high performance disk I/O systems,” US Patent and Trademark Office, PTO No. 5,754,888. (with Yiming Hu)
3. “RAPID-Cache (Redundant, Asymmetrically Parallel, Inexpensive Disk Cache), A new cache structure for RAID systems,” U.S. Patent and Trademark Office, No. 6,243,795, June 5th, 2001. (with Yiming Hu)
4. “STICS--SCSI-To-IP Cache Storage,” US Patent and Trademark Office, US Patent No. 7,275,134. (with Xubin He).
5. “RORIB--A cost effective approach for real-time, online and remote information backup,” US Patent No. 7,177,887. (with Jian Li).
6. “Cache architecture for a processing unit providing reduced power consumption in cache operation” U.S. Patent No. 7,966,452.
7. “Data Recovery System and Method including a Disk Array Architecture that Provides Recovery of Data to Any Point of Time” U.S. Patent No. 7,730,347.
8. “ACE: Adaptive cache engine for storage area network including systems and methods related thereto” United States Patent No. 7,370,163. Issued on May 6, 2008. (with Ming Zhang and Yinan Liu)
9. “Data replication method over a limited bandwidth network by mirroring parities,” U.S. Patent 7,457,980.
10. “SWEET: System and Method for Maintaining Redundant Storages Coherent using Sliding Window of Eager Execution Transactions (SWEET),” US Patent No. 8,140,772.
11. “HELP---Hardware Environment for Low-overhead Profiling/Optimization and Security Functions,” US Patent and Trademark Office Pending, File #7378.
12. “BUCS—Bottom Up Cache Structure for networked storage servers,” Patent Application Filed with US Patent and Trademark Office on Oct. 20, 2003. Serial Number 60/512,728.
13. “CUP: Coupling Update by Parities, A method and apparatus for maximizing data recovery,” Application No. 60/940,831.
14. “APS: Method and Apparatus for Approximate Positioning System in Personal Area Networks Using ZigBee” Application filed on March 28, 2006. (with Yan Sun, W. Xiao, and Y. Liu)
15. “Methods for detecting unfair ratings and building trust in raters in online rating systems using signal modeling technique” Application Pending: 60/894,012, ( with Yan Sun)
16. “RINGS: Recover Information from NAND Gates Storages”, US Patent and Trademark Office, Filed in May 2008. Co-inventor: Weijun Xiao

## **PUBLICATIONS**

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## **REFERENCED CONFERENCE PAPERS**

1. Jin Ren and Qing Yang "I-CASH: Intelligently Coupled Array of SSD and HDD" in The 17th IEEE International Symposium on High Performance Computer Architecture, 2011 (HPCA'11), San Antonio, TX, Feb 2011.
2. Fan Zhang, Will DiSanto, Jin Ren, Zhi Dou, Qing Yang, and He Huang, "A Novel CPS System for Evaluating a Neural-Machine Interface for Artificial Legs" ACM/IEEE Second International Conference on Cyber-Physical Systems, Chicago, April 12 - 14, 2011.
3. Jin Ren and Qing Yang A New Buffer Cache Design Exploiting both Temporal and Content Localities *The 30th International Conference on Distributed Computing Systems, ICDCS 2010*. Genoa, Italy, June 21-25, 2010.
4. Jiguang Wan, Jibin Wang, Qing Yang, and Changsheng Xie, "S2-RAID: A New RAID Architecture for Fast Data Recovery" *Proceedings of 26th IEEE Symposium on Massive Storage Systems and Technologies*, Lake Tahoe, Incline Village, Nevada, May 3-7, 2010
5. He Huang, Yan (Lindsay) Sun, Qing Yang, Fan Zhang, Xiaorong Zhang, Yuhong Liu, Jin Ren, Fabian Sierra. "Integrating Neuromuscular and Cyber Systems for Neural Control of Artificial Legs" *ACM/IEEE International Conference on Cyber-Physical Systems* Stockholm, Sweden. April, 2010
6. Qing Yang "Secure and Efficient Data Replay in Distributed eHealthcare Information System", *International Conference on Information Society (i-Society 2010)* June 28-30, 2010, London, UK.
7. Yang, Y., Sun, Y. L., Kay, S., and Yang, Q. 2009. Defending online reputation systems against collaborative unfair raters through signal modeling and trust. In *Proceedings of the 2009 ACM Symposium on Applied Computing (Honolulu, Hawaii)*. SAC '09. ACM, New York, NY, 1308-1315. DOI= <http://doi.acm.org/10.1145/1529282.1529575>
8. Weijun Xiao and Qing Yang, "A Case for Continuous Data Protection at Block Level in Disk Array Storages" *IEEE Transactions on Parallel and Distributed Systems, Volume 20, Issue 6 (June 2009), Pages 898-911*.
9. Weijun Xiao, Qing Yang, J. Ren, C. Xie, and H. Li, "Design and Analysis of Block Level Snapshots for Data Protection and Recovery" *IEEE Trans. Comput.* 58, 12 (Dec. 2009), 1615-1625. DOI= <http://dx.doi.org/10.1109/TC.2009.107>
10. Weijun Xiao and Qing Yang, "Can We Really Recover Data If Storage Subsystem Fails?" *The 28th International Conference on Distributed Computing Systems*, Beijing, China, 2008. (ICDCS'08).
11. X. Li, Changsheng Xie, and Qing Yang, "Optimal Implementation of Continuous Data Protection (CDP) in Linux Kernel," *Proc. Of IEEE Int'l Conference on Networking, Architecture, and Storage*, Chongqing, China, June 2008.
12. Yafei Yang, Yan Lindsay Sun, Jin Ren, and Qing Yang, "Building Trust in Online Rating Systems Through Signal Modeling," *International Workshop on Trust and Reputation Management in Massively Distributed Computing Systems, June 25-29, 2007, in conjunction with ICDCS 2007*
13. Qing Yang, Weijun Xiao, and Jin Ren , "TRAP-Array: A Disk Array Architecture Providing Timely Recovery to Any Point-in -time" in The 33rd Annual International Symposium on Computer Architecture, 2006 (ISCA'06).
14. Qing Yang, Weijun Xiao, and Jin Ren , "PRINS: Optimizing Performance of Reliable Internet Storages" *The 26th International Conference on Distributed Computing Systems*, Lisbon, Portugal, 2006. (ICDCS'06).
15. W. Xiao, Y. Liu, Qing Yang, J. Ren, and C. Xie. "Implementation and Performance Evaluation of Two Snapshot Methods on iSCSI Target Storages" in *NASA/IEEE 14th Conf. on Mass Storage Systems and Technologies*, College Park, Maryland, May 2006

16. Qing Yang "On Performance of Parallel iSCSI Protocol for Networked Storage Systems" in IEEE 20<sup>th</sup> Int'l Conf on Advanced Information Networking and Applications, Vienna, Austria, April 2006.
17. Weijun Xiao; Yan Sun; Yinan Liu; Qing Yang, "TEA: Transmission Error Approximation for Distance Estimation between Two Zigbee Devices" NAS (Networking, Architecture, and Storage) 2006.
18. Ming Zhang and Qing Yang, "BUCS - A Bottom-Up Cache Structure for Networked Storage Servers", International Conference on Parallel Processing., Montreal, Canada, Aug, 2004, pp.310-317.
19. Ming Zhang, Yinan Liu, and Qing Yang, "Cost-Effective Remote Mirroring Using the iSCSI Protocol", 21st IEEE Conference on Mass Storage Systems and Technologies, April, 2004, pp.385-398.
20. Ming Zhang, Qing Yang, and Xubin He, "SPEK: A Storage Performance Evaluation Kernel Module for Block Level Storage Systems", in *Proceedings of 11<sup>th</sup> IEEE/ACM International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS)*, Orlando, October 12-15, 2003.
21. Ming Zhang, Xubin He, and Qing Yang, "A Unified, Low-overhead Framework to Support Continuous Profiling and Optimization", Proc. Of IEEE IPCCC 2003, Apr, 2003.
22. Ming Zhang and Qing Yang, "Evaluating Availability of Networked Storages Using Commercial Workload", presented at *Sixth Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW)*, Feb, 2003.
23. Ming Zhang and Qing Yang, "N-SPEK: A Performability Benchmark Tool for Networked Storage Systems", to be presented at *Workshop on Parallel I/O in Cluster Computing and Computational Grids.*, 12-15 May 2003, Toshi Center Hotel, Tokyo, JAPAN
24. Xubin He, Qing Yang, and Ming Zhang, "A Caching Strategy to Improve iSCSI Performance," in *Proc. of IEEE Annual Conference on Local Computer Networks*, Nov. 6-8, 2002.
25. Xubin He, Qing Yang, and Ming Zhang, "Introducing SCSI-To-IP Cache for Storage Area Networks", *IEEE International conference on Parallel Processing (ICPP'2002)*, August 2002, pp. 203-210
26. Ming Zhang, Xubin He, and Qing Yang, "Implementation and Performance Evaluation of RAPID-Cache under Linux," *Proc. of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'2002)*, June 2002.
27. Ming Zhang and Xubin He, "A Unified, Low-overhead Framework to Support Continuous Profiling and Optimization", to appear in *Proceedings of 22nd IEEE International Performance Computing and Communications Conference (IPCCC'2003)*, Phoenix, Arizona, April 2003.
28. Xubin He, Ming Zhang, and Qing Yang, "DRALIC: A Peer-to-Peer Storage Architecture" *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'2001)*, Volume II, June 2001, pp. 908-913.
29. Xubin He and Qing Yang, "Characterizing the Home Pages" *Proceedings of the 2nd International Conference on Internet Computing (IC'2001)*, June 2001, pp. 976-982.
30. Xubin He and Qing Yang, "VC-RAID: A Large Virtual NVRAM Cache for Software Do-it-yourself RAID" *Proceedings of the International Symposium on Information Systems and Engineering (ISE'2001)*, June 2001, pp.334-340.
31. Xubin He and Qing Yang, "Performance evaluation of distributed web servers under commercial workload" in *Proceedings of Internet Conference'2000*, Las Vegas
32. Xubin He and Qing Yang, "A DCD Filter Driver for Windows NT 4" *Proceedings of the 12th International Conference on Computer Applications in Industry and Engineering (CAINE-99)*, Atlanta, Georgia, USA, Nov. 4-6, 1999.
33. Yiming Hu, Ashwini Nanda and Qing Yang, "Measurement, Analysis and Performance Improvement of the Apache Web Server", in the *18th IEEE International Performance*,

*Computing and Communications Conference (IPCCC'99)*, Phoenix/Scottsdale, Arizona, February 1999.

34. T. Nightingale, Y. Hu, and Qing Yang, "Design and Implementation of a DCD Device Driver for Unix", in *Proceedings of the 1999 USENIX Annual Technical Conference*, Monterey, California, June 1999.
35. Y. Hu, Q. Yang, and T. Nightingale, "RAPID-Cache --- A Reliable and Inexpensive Write Cache for Disk I/O Systems", in the *5th International Symposium on High Performance Computer Architecture (HPCA-5)*. Orlando, Florida. Jan. 1999.
36. Y. Hu and Q. Yang, "DCD---Disk Caching Disk: A New Approach for Boosting I/O Performance," *23rd Annual International Symposium on Computer Architecture*, Philadelphia PA May, 1996.
37. H. Wang, T. Sun, and Q. Yang, "Caching Address Tags: A technique to reduce chip area cost for on-chip caches," *22nd Annual International Symposium on Computer Architecture*, Santa Margherita Ligure, Italy, June, 1995.
38. Q. Yang and Liping W. Yang, "A novel cache design for vector processing," *Proc. of 19th Int'l Symp. on Computer Architecture*, May 1992, pp. 362-371.
39. Li Yang, X. Pei, and Qing Yang "Performance Analysis of A new Disk Architecture as A Netserver for NFS Network Systems", *Int'l Conference on Computer Applications in Industry and Engineering (CAINE-96)*, Dec. 1996.
40. T. Sun and Q. Yang, "Evaluating cache performance for vector computers," In *Proc. Int'l Conf. on Parallel and Distributed Computing*, Oct. 1994
41. Chenyi Hu, Baker Kearfott, Joe Sheldon and Qing Yang, "Solving nonlinear systems on vector supercomputers," In *Proc. Int'l Conf. on Parallel and Distributed Computing*, Oct. 1994.
42. Sibabrata Ray, Hong Jiang and Qing Yang, "A New Approach To Network Latency Reduction of Multiprocessors by Data Migration in The Absence of Cache Coherence Mechanisms" In *Proc. ISCA Int'l Conf. on Parallel and Distributed Computing*, Oct. 1994.
43. N. Annupindi, M. An, J. W. Cooley and Qing Yang, "A new and efficient FFT algorithm for distributed memory systems," in *Proceedings of International Conference on Parallel and Distributed Systems*, Dec. 1994, Taiwan
44. T. Sun and Q. Yang, "A comparison of cached and uncached vector computers," in *Proceedings of IEEE 1994 Int'l Conf. on Parallel and Distributed Systems*, Oct. 1994.
45. Tao Yang, Shengbin Hu and Qing Yang, "A closed form formula for queueing delays in disk arrays," *Proceedings of 94' Int'l Conf. on Parallel Processing*, Aug. 1994.
46. Q. Yang and S. Adina, "A one's complement cache," *Proceedings of 94' Int'l Conf. on Parallel Processing*, Aug. 1994.
47. H. Wang and Q. Yang, "On fault tolerant computation of orthogonal transforms on hypercube multiprocessors," In *Proc. of 21th Int'l Conf. on Parallel Processing*, Vol. 1, Aug. 1992.
48. Q. Yang, "Effects of arbitration protocols on the performance of multiple-bus multiprocessors," In *Proc. of 20th Int'l Conf. on Parallel Processing*, Vol. 1, 1991.
49. H. Wang and Q. Yang, "A Prime-Cube graph approach for processor allocation in hypercube multiprocessors," In *Proc. of 20th Int'l Conf. on Parallel Processing*, Vol. 1, pp. 25-32, 1991
50. Qing Yang and X. Qian, "Load balancing on distributed multiprocessor architectures with LAL", in *Proc. on 11th Int'l Conf. on Distributed Computing Systems*, May 1991, pp. 402-409.
51. C. Hu, M. Bayoumi, B. Kearfott and Q. Yang, "A parallelized algorithm for the preconditioned interval Newton method," *Proc. 5th SIAM Conf. on Parallel Processing*, March, 1991
52. Q. Yang, G. Thangadurai and L. N. Bhuyan, "An adaptive cache coherence scheme for hierarchical shared-memory multiprocessors," *IEEE Symp. on Parallel Processing*, Dec. 1990.
53. Qing Yang and R. Ravi, "Design and analysis of multiple-bus arbiters with different priority schemes", in *Proc. of PARBASE-90--Int. Conf. on Database, Parallel Architectures, and Their Applications*, pp 238-247 March, 1990

54. Q. Yang, "On performance improvement of cache coherence protocols for hierarchical multiprocessors," *ISMM Int'l Conf. on Parallel and Distributed Computing, and Systems*, Oct. 1990.
55. Qing Yang, "Performance analysis of a cache coherent multiprocessor based on hierarchical buses", in *Proc. of PARBASE-90-Int. Conf. on Database, Parallel Architectures, and Their Applications*, pp 248-257 March, 1990.
56. Q. Yang and L.N. Bhuyan, "A queueing network model for cache coherence protocol on asynchronous multiple-bus multiprocessors," in *88'Int'l Conf. on Parallel Processing*, pp. 130-137, 1988.
57. Q. Yang, L.N. Bhuyan, and R. Pavaskar, "Performance analysis of packet switched multiple-bus multiprocessor systems," in *Proceedings of Eighth Real-Time System Symposium*, Dec. 1987, pp. 170-178.
58. Q. Yang and L.N. Bhuyan, "Design and analysis of decentralized multiple-bus multiprocessor," in *Proceedings of 87'Int'l Conf. on Parallel Processing*, Aug. 1987, pp. 889-892
59. Q. Yang, D. Ghosal and L.N. Bhuyan, "Analysis of Multiple Token-ring and Multiple Slotted-ring Networks," *IEEE Proceedings Computer Networking Symposium*, Washington D.C., Nov. 1986, pp 79-86.
60. Q. Yang, D. Ghosal and L.N. Bhuyan, "Design and analysis of multiple-ring networks for distributed processing," In TR 86-3-1, CACS, USL, 1986.
61. Qing Yang, D. Ghosal, and S. K. Tripathi, "Performance study of two protocols for data/voice intergration on ring networks," UMIACS-TR-90-46, Univ. of Maryland, 1990.
62. Yiming Hu, Ashwini Nanda and Qing Yang, "Profiling and performance enhancement of Appache web servers," Tech. Report, URI

## JOURNAL PAPERS

63. Zhang, X.; Liu, Y.; Zhang, F.; Ren, J.; Sun, Y.; Yang, Q.; Huang, H.; On Design and Implementation of Neural-Machine Interface for Artificial Legs, in: *Industrial Informatics*, IEEE Transactions on, Digital Object Identifier: 10.1109/TII.2011.2166770 Date of Publication: 06 September 2011.
64. J. Yang, Q. Cao, X. Li, C. Xie, and Q. Yang "ST-CDP: Snapshots in TRAP for Continuous Data Protection," *IEEE Trans. On Computes*, <http://doi.ieeecomputersociety.org/10.1109/TC.2011.150>
65. Jin Ren and Qing Yang, "BLUVS: A Block Level Unlimited Versioning System," Submitted to *IEEE Transaction on Computers*.
66. Weijun Xiao, Qing Yang, Jin Ren, Changsheng Xie, and Huaiyang Li, "Design and Analysis of Block Level Snapshots for Data Protection and Recovery," *IEEE Transaction on Computer*, 58, 12 (Dec. 2009), 1615-1625..
67. Weijun Xiao, Jin Ren, and Qing Yang, "A Case for Continuous Data Protection at Block Level in Disk Array Storages," *IEEE Transaction on Parallel and Distributed Systems*, Volume 20, Issue 6 (June 2009), Pages 898-911.
68. Weijun Xiao, Yan Sun, Yinan Liu, and Qing Yang, "TEA: Transmission Error Approximation for distance estimation between two Zigbee devices," *Int. J. High Performance Computing and Networking*, 2008, to appear.
69. Xubin He, Ming Zhang, and Qing Yang, "SPEK: A storage performance evaluation kernel module for block level storage systems under faulty conditions" *IEEE Transaction on Dependable and Secture Computing* , Vol. 2, No. 2, April-June 2005, pp. 138-149.
70. Xubin He, Ming Zhang, and Qing Yang, "STICS: SCSI-To-IP Cache for Storage Area Networks", *Journal of Parallel and Distributed Computing* , vol. 64, No. 9, pp. 1069-1085, September 2004.

71. Scott Lloyd, Jian Li, Joan Peckham, and Qing Yang, "RORIB, An economic and efficient solution for Real-time, Online, Remote Information Backup," in *Journal of Database Management, JDM S00-294, Vol. 14, No. 3, July-Sept. 2003, pp. 56-73.*
72. Y. Hu, T. Nightingale and Q. Yang, "RAPID-Cache --- A Reliable and Inexpensive Write Cache for High Performance Storage Systems", *IEEE Transactions on Parallel and Distributed Systems*, Vol. 13, No. 3. March 2002, pp.290-307.
73. Xubin He and Qing Yang "Performance Evaluation of Distributed Web Server Architectures under E-Commerce Workloads" Submitted to *Journal of Parallel and Distributed Computing*.
74. Xubin He, Ming Zhang, and Qing Yang, "STICS: SCSI-To-IP Cache for Storage Area Networks," Submitted to *IEEE Transactions on Parallel and Distributed Systems*.
75. Yiming Hu, Ashwini Nanda and Qing Yang, "Measurement, Analysis and Performance Improvement of the Apache Web Server", *International Journal of Computers and Their Applications*, Vol. 8, No. 4, Dec. 2001.
76. Xubin He and Qing Yang "On Design and Implementation of a Large Virtual NVRAM Cache for Software RAID", in *Special Issue of Calculateurs Parallel Journal on Parallel I/O for Cluster Computing, 2002 spring*.
77. Y. Hu and Q. Yang, "A New Hierarchical Disk Architecture", *IEEE Micro, Vol. 18, No. 6, Nov/Dec. 1998.*
78. T. Sun and Q. Yang, "A comparative analysis of cache memories for vector processing," in *IEEE Trans. on Computers, Vol. 48, No.3 March 1999, pp. 331-344.*
79. Li Yang, X. Pei, and Qing Yang "Performance Analysis of A new Disk Architecture as A Netserver for NFS Network Systems", in *Int'l Journal on Computers and Their Applications*, Vol. 6, No. 3, Sept. 1999, pp. 159-165.
80. H. Wang, T. Sun, and Q. Yang, "Minimizing area cost of on-chip cache memories by caching address tags", *In IEEE Trans. on Computers*, Vol. 46, No. 11. Nov. 1997, pp. 1187-1201.
81. Q. Yang, Sridah Adina and T. Sun, "Designing on-chip cache using complement numbers", in *Journal of Parallel and Distributed Computing*, Academic Press. Vol. 48, pp. 143-164, 1998
82. Qing Yang and Tao Yang, "A memory interference model for regularly patterned multiple stream vector accesses," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 6, No. 5, pp. 520-530, May 1995.
83. Qing Yang, "Introducing a new cache design into vector computers," in *IEEE Transactions on Computers*, Vol. 42, No. 12, Dec. 1993, pp. 1411-1424. The Prime-mapped Cache
84. Nagesh Anupindi, Qing Yang and M. An, "Tensor Product Formulations of Data Partition and Migration for Matrix Transpose and FFT Algorithms", in *Journal of Parallel and Distributed Computing*.
85. S. Ray, H. Jiang and Q. Yang, "A Compiler-directed Approach to Network Latency Reduction in Distributed Shared Memory Multiprocessors", *Journal of Parallel and Distributed Computing*, Special Issue on Compilation Techniques for Distributed Memory Systems
86. C-M Chung, D-A Chiang and Qing Yang "A comparative analysis of different arbitration protocols for multiple-bus multiprocessors" *International Journal of Computer Science and Enigeering*. Vol. 11, No. 3, May 1996.
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91. Qing Yang, "Performance of cache memories for vector computers," in *Journal of Parallel and Distributed Computing*, Special Issue on Performance of Supercomputers. 19 pp.163-178, 1993.
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93. Qing Yang and H. Wang, "A graph approach to minimizing processor fragmentations on hypercube multiprocessors", in *IEEE Transactions on Parallel and Distributed Systems*, Oct. 1993, pp. 1165-1171.
94. Qing Yang, D. Ghosal, and S. K. Tripathi, "Performance study of two protocols for voice/data integration on ring networks", in *Computer Networks and ISDN* Vol. 23, 1992, pp. 267-285.
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97. Qing Yang and L. N. Bhuyan, "Performance of Multiple-Bus Interconnections for Multiprocessors," in *Journal of Parallel and Distributed Computing*, 8, pp. 267-273 (1990).
98. Qing Yang, L. N. Bhuyan and B. Liu, "Analysis and Comparison of Cache Coherence Protocols for a Packet-Switched Multiprocessor," in *IEEE Transactions on Computers*, Special Issue on Distributed Computer Systems, Aug. 1989, pp 1143-1153.
99. L. N. Bhuyan, D. Ghosal, and Qing Yang, "Approximate Analysis of Single and Multiple-ring Networks," in *IEEE Transactions on Computers*, July 1989, pp 1027-1040.
100. L. N. Bhuyan, Qing Yang and D. P. Agrawal, "Performance of Multiprocessor Interconnection Networks", *IEEE Computer*, vol. 22, No. 2, pp.25-37, Feb. 1989.
101. Qing Yang and S. G. Zaky, "Communication performance in multiple-bus systems", *IEEE Transactions on Computers*, Vol. 32, No. 7, pp. 848-853, July 1988.

## BOOK CHAPTERS

102. Scott J. Lloyd, Joan Peckham, Jian Li and Qing (Ken) Yang, "Simultaneous Database Backup Using TCP/IP and Specialized Network Interface Card," Chapter IV, *Advanced Topics in Database Research*, Vol. 4, IGP: Idea Group Publishing
103. Xubin He, Qing Yang, "A Large Virtual NVRAM Cache for Software RAID," *Parallel I/O for Cluster Computing (Chapter 7)*, Editors: Christophe CÉRIN and Hai JIN, 2002 September.
104. Chapter 15: RAPID-Cache --- A Reliable and Inexpensive Write Cache for Disk I/O Systems , in Hai Jin, Toni Cortes, and Rajkumar Buyya (editors), *High Performance Mass Storage and Parallel I/O: Technologies and Applications*, IEEE & Wiley Press, ISBN 0-471-20809-4, New York, USA, 2001.
105. L. N. Bhuyan, D. Ghosal, Q. Yang "Approximate analysis of single and multiple ring networks", in *Fiber Optic Local Area Networks*, Ed: Eric G. Rawson, SPIE Press, 1990.
106. Qing Yang, "Performance analysis of a cache coherent multiprocessor based on hierarchical buses", in *Parallel Architectures*, Ed: N. Rische, S. Navathe and D. Tal, IEEE Computer Society Press, 1990.
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109. Qing Yang, "Processor allocation in multicomputers," in *Practical Aspects of Parallel Computing*, Ed: L. Tao, 1994.
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## RESEARCH GRANTS AND CONTRACTS

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1. Qing Yang, "Introducing I-CASH, A New Disk IO Architecture", THE NATIONAL SCIENCE FOUNDATION, CCF - SOFTWARE & HARDWARE FOUNDATION CCF-1017177, Aug. 1 2010 - July 31, 2014. PI, 1 of 1. Qing Yang, "Towards Neural-controlled Artificial Legs using High-Performance Embedded Computers", \$1.38Million, NSF-CISE Cyber Physical System Program, September 2009-Sept. 2013. with He Huang and Yan Sun
3. Qing Yang, "Design of a Real-Time Fusion-based Neural Controlled Artificial Legs" National Institutes of Health, R21, with He Huang .
4. Qing Yang, "Understanding, Analyzing, and Designing Storage Subsystem Architectures for Maximum Data Recoverability," National Science Foundation, Aug. 1, 2008 to Aug. 1, 2011. Principal Investigator, 1 of 1.
5. Qing Yang, "Validation and Evaluation of a New Data Replication Technology," National Science Foundation, SGER Grant, Feb. 2006 to July 2007.
6. Qing Yang and B. Nassersharif , "Reshaping computer engineering education and training for the information era," NASA NNX06AB10G, Sept. 2006-Sept 2008. (PI)
7. Qing Yang, "Design and Analysis of Data Processing and Storage in Image Processing Systems," NI, Aug. 1, 2007 to Sept. 2008. Principal Investigator, 1 of 1.
8. Qing Yang, "HELP - A Profiling Tool for Disk I/O and Networked Storage," National Science Foundation, CCR-0312613, ITR grant, Aug. 2003 to July 2006. Principal Investigator 1 of 1.
9. Qing Yang, "Boosting Webserver Performance Using DRALIC----Distributed RAID and Location Independence Caching", National Science Foundation, 3 years, Sept. 2000 to Sept. 2003, Principal Investigator 1 of 1.
10. Qing Yang, "A New Spectrum of Hierarchical Storage Architectures for High Performance Disk I/Os." National Science Foundation, Grant No. MIP-9714370, (PI 1 of 1).
11. Qing Yang, "Exploring design space for high performance low cost memory hierarchy," National Science Foundation Grant No. MIP-9505601, Aug. 1995-Aug. 1998. Principal Investigator (1 of 1).
12. Qing Yang, "Introducing a new cache design into vector computers," National Science Foundation Grant No. MIP-9208041, three years from June 1992 to Dec. 1995, Principal Investigator (1 of 1).
13. Qing Yang, "Design and analysis of high performance cache-coherent multiprocessors based on shared buses", National Science Foundation grant CCR-8909672, Aug. 1989 - July 1992, Principal Investigator (Research Initiation Award).
14. "Equipment for diverse computer architecture research" National Science Foundation, Jan. 1998-Jan. 1999, co-PI with Gus Uht, Don Tufts, J-C. Lo.
15. Qing Yang "Effects of disk accesses on the performance of computer systems",NSF, November 1996 - June 1997.
16. "Evaluating Web Server performance on multiprocessors", IBM December 1996 --December 1997,
17. Qing Yang "Prototyping DCD", URI Research Council.
18. Qing Yang "Research Experience for Undergraduates", National Science Foundation, Aug. 1996 - July 1998. Principal Investigator.

19. Qing Yang, "Optimization of Parallel Computing on Cache-Coherent Multiprocessor", Research Council Grant for July 1991-July 1992, Principal Investigator
20. Travel grant from National Science Foundation for to present a paper at ISCA92 in Australia.
21. Qing Yang, "Innovative architecture designs for supercomputers," URI Research Council for Aug. 1992 - Dec. 1992., Principal Investigator
22. Qing Yang, "Upgrading Computer Organization Lab," Intel Corp. April 1993, Principal Investigator.
23. Qing Yang, United Nation Industrial Development Organization, UNIDO, Training In ternational scholars May 1993
24. Qing Yang, United Nation Industrial Development Organization, UNIDO, Training In ternational scholars May 1994.
25. Qing Yang, "Computer Applications in Industry," Xifeng Industrial Inc.

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## **GRADUATE STUDENTS ADVISED**

### **PH.D. GRADUATES**

1. Jin Ren, Ph.D, Jan. 2011, Senior software architect, VeloBit, Inc.
2. Weijun Xiao, Ph.D, May 2009. Named as Computing Innovation Fellow by the Computing Community Consortium (CCC) and the Computing Research Association (CRA) funded by NSF
3. Ming Zhang, May, 2005, Senior Research Architect, Tandberg Co.
4. Xubin Ben He, Ph.D, July 2002, Tenured Assoc. Professor, Department of Electrical and Computer Engineering, Tennessee Technological University
5. Yiming Hu, Ph.D, Jan. 1999, Tenured Assoc. Prof. U. of Cincinnati, winner of NSF 2000' Career Award.
6. Hong Wang, Ph.D, Jan. 1996, Director of Intel Microprocessor Research Lab. Senior Principal Researcher (Sr. Principal Engineer), Intel Co. Winner of 1999 Intel Accomplishment Award.
7. Nagesh Anupindi, 1994, Senior Scientist, Aware Inc., Cambridge, MA
8. Tong Sun, 1996, Principle Scientist, Xerox Co., Rochester, New York

### **MASTER GRADUATES**

Kurt R. Almquist, George Thangadurai, Ravi Raja, Qi Gan, V. Geetha, J. Huang, Adina Sridha, Kevin Yee, Gregory Bussiere, Jie Lu, Xiaosong He, Brian Capoccia, John Didier, Jian Li, Yaodong Hu.

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## **PROFESSIONAL ACTIVITIES**

- IEEE Fellow
- General Chair, International Symposium on Computer Architecture, 2011, (the premier conference in the field)
- Co-Founder and Chair for IEEE International Conference on Networking, Architecture and Storages. Successfully held for 5 consecutive years.
- Program Committee Member: International Symposium on High Performance Computer Architecture, 2006
- Program Committee Member: IEEE International Symposium on Workload Characterization, 2005,
- Program Committee Member: International Symposium on Computer Architecture and High Performance Computing, 2005, SBAC-PAD05
- Program Committee Member: IFIP International Conference on Network and Parallel Computing 2005

- Founder and Workshop Chair, International Workshop on Storage Network Architecture and Parallel I/Os, SNAPI'05. SNAPI has been successfully held annually for 4 years.
- Served in two NSF Panels in 2005.
- Associate Editor, IEEE Transaction on Parallel and Distributed Systems, 1999-2001.
- Membership Chair, IEEE TCCA, 2002-present.
- Distinguished Speaker of IEEE Computer Society, 1996-1999.
- Program Committee Chairman, Int'l Conf. On Computer Applications in Industry and Engineering, Nov. 1999
- Program Committee Chairman, International Workshop on High Performance Computing, Beijing China, 1995
- Publication Chairman, International Symposium on High Performance Computer Architecture 1995
- Program Committee Members of several international conferences.
- Guest editor of several professional journals.
- Invited speaker for numerous universities and companies in the world.
- Referees for several professional journals.

### **PERSONAL INFORMATION**

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Married with two daughters and two sons. Love Tennis, badminton, and boating.