Ideal and Resistive Nanowire Decoders

General Models for Nanowire Addressing

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February 03, 2006
The Nanowire

- Sets of parallel NWs have been produced.
- Devices will reside at NW intersections.
- We must gain control over individual NWs.

SNAP NWs (Heath, Caltech)   CVD NWs (Lieber, Harvard)   Directed Growth (Stoykovich, UW)
The Crossbar

The crossbar is currently the most feasible nano-scale architecture.

By addressing individual NWs, we can control programmable molecules at NW crosspoints.

Crossbars are a basis for memories and circuits.
Nanowire Control

- Mesoscale contacts apply a potential along the lengths of NWs.
- Mesoscale wires (MWs) apply fields to across NWs, some of which form FETs.
- NW/MW junctions can form FETs using a variety of technologies:
  - Modulation-doping
  - Random Particle deposition
  - Masking NWs with dielectric material
Simple NW Decoders

- A potential is applied along the NWs.
- $M$ MW inputs control $N$ NW outputs. Each MW controls a subset of NWs.
- When a MW produces a field, the current in each NW it controls is greatly reduced.
- Each MW “subtracts” out subsets of NWs. This permits $M << N$.
- Decoders are assembled stochastically and are difficult to produce if $N$ large.
Composite Decoders

- A composite decoder uses multiple simple decoders to control many NWs.
- The simple decoders share MW inputs.
- This space savings allows for mesoscale inputs.
Ideal Decoders

- To analyze a decoder, we must model how MWs control NWs.
- In an ideal decoder, a MW’s electric field completely turns off the NWs it controls. Other NWs are unaffected.
- This model is accurate if the FETs formed from MW/NW junctions have high on/off ratios.
Binary Codewords

- In an ideal decoder, we associate an $M$-bit codeword, $c_i$, with each NW, $n_i$.
- The $j^{th}$ MW controls the $i^{th}$ NW if and only if the $j^{th}$ bit of $c_i$, $c_{ij}$, is 1.
- The $M$-bit decoder input, $A$, causes $n_i$ to carry a current if and only if $A \cdot c_i = 0$.
- Codeword assignment is stochastic.
- Control over codewords is a key way to compare decoding technologies.
Codeword Interaction

- If $c_{bj} = 1$ where $c_{aj} = 1$, $c_a$ implies $c_b$. Inputs that turn off $n_a$ turn off $n_b$.

- A set of codewords, $S$, is addressable if some input turns off all NWs not in $S$.

- $S = \{c_i\}$ is addressable if and only if no codeword implies $c_i$. $S$ is addressed with input $A = c_i$. 
Decoders for Memories

• A $B$-bit memory maps $B$ addresses to $B$ disjoint sets of storage devices.

• A $D$-address memory decoder addresses $D$ disjoint subsets of NWs.

• Equivalently, the decoder contains $D$ addressable codewords.
Resistive Decoders

- Decoders that rely on FETs are not ideal.
- MWs carrying a field increase each NW’s resistance by some amount.
- In a resistive decoder, codewords are real-valued. In real-valued codeword $r_i$, $r_{ij}$ is the resistance induced in $n_i$ by the $j^{th}$ MW.
- On input $A$, $n_i$’s resistance is $r_{base} + A \cdot r_i$. 
Ideal vs. Resistive

- In a resistive memory decoder the addressed NWs must output more current than the other NWs.

- Consider 1-hot codewords:
  \[ \Rightarrow \text{The addressed wire has resistance} < r_{\text{base}} + Mr_{\text{low}} \]
  \[ \Rightarrow \text{Remaining wires have resistance} > (r_{\text{base}} + r_{\text{high}})/N \]

- We require that \( r_{\text{high}} \gg MNr_{\text{low}} \) and \( Nr_{\text{base}} \)
  - If \( r_{ij} \leq r_{\text{low}} \), \( c_{ij} = 0 \).
  - If \( r_{ij} \geq r_{\text{high}} \), \( c_{ij} = 1 \).
  - If \( r_{\text{low}} < r_{ij} < r_{\text{high}} \), \( c_{ij} \) is an error.
Ideal Decoders with Errors

- To apply the ideal model to resistive decoders, consider binary codewords with random errors.
- If $c_{ij} = e$, the $j^{th}$ MW increases $n_i$'s resistance by an unknown amount.
- Consider input $A$ such that the $j^{th}$ MW carries a field. $A$ functions reliably if a MW for which $c_{ik} = 1$ carries a field.
Balanced Hamming Distance

- Consider two error-free codewords, $c_a$ and $c_b$. Let $|c_a - c_b|$ denote the number of inputs for which $c_{aj} = 1$ and $c_{bj} = 0$.

- The balanced Hamming distance (BHD) between $c_a$ and $c_b$ is $2 \cdot \min(|c_a - c_b|, |c_b - c_a|)$.

- If $c_a$ and $c_b$ have a BHD of $2d + 2$ they can collectively tolerate up to $d$ errors.
Fault-Tolerant Random Particle Decoders

- In a particle deposition decoder, \( c_{ij} = 1 \) with some fixed probability, \( p \).

- If each pair of codeword has a BHD of at least \( 2d + 2 \), the decoder can tolerate \( d \) errors per pair.

- This holds with probability \( > 1 - f \) when

\[
M > \frac{(d + (d^2 + 4 \ln(N^2/f))^{1/2})^2}{4p(1 - p)}
\]
Conclusion

• Any nanoscale architecture will require control over individual NWs.

• Stochastically assembled decoders can provide reliable control even if errors occur.

• Our decoder model applies to many viable technologies and provides conditions that decoders must meet.