

ELE 201 – Digital Circuit Design

Fall 2002

Catalog Description: Logic gates, Boolean algebra, combinatorial and sequential circuits, analysis and design of sequential systems, multi-input system controllers, asynchronous finite state machines.

Course Objectives:

To understand the basic ideas and methods used in designing digital systems for later use in advanced courses on digital circuit design, computer hardware, and computer architecture. To understand and use a hierarchical approach to the design of complicated systems.

To question the use of algorithmic solutions to problems, to grasp when they can be useful and when they are inadequate.

To design digital circuits up to the level of using medium scale integrated circuit chips.

Schedule: Monday, Wednesday & Friday 9:00-9:50, Cherry Auditorium, Kirk

Instructor: Prof. Peter F. Swaszek, 119 Kelley Annex, URI
swaszek@ele.uri.edu or (401) 874-5802 (try e-mail first!)
office hours (typical): Monday 10-11, 1-2; Tuesday 8:30-9:15,
Wednesday 8-9, 10-11, Friday 10-11, and by
appointment

Course Text: *Digital Design – Principles and Practices*, by J. F. Wakerly, Prentice Hall

Topics: (chapters 1, 2, 4-10 of Wakerly, but not in order!)

Introduction – digital concepts, binary representations

Combinational logic – gates, Boolean algebra, Karnaugh maps, standard forms for Boolean expressions using NAND, NOR, and EXOR gates,

Sequential circuits – Latches, D, JK, and T flip-flops, synchronous sequential circuit analysis and design, registers and counters, finite-state machine design

Math circuits – number systems, arithmetic operations, codes

MSI chips – decoders, encoders, and multiplexers, arithmetic circuits

Memory and programmable logic devices – random access memory, error detection and correction, ROM, PLA, PAL, FPGA

Grading: 10 quizzes 40%
Midterm exam 25%
Final exam 35%

Tentative Semester Schedule

Week	Dates	Lecture topics	Chapters
1	9/4	Course introduction, introduction to digital circuits	1
	9/6	Combinational circuits, truth tables, AND, OR, NOT gates, timing diagrams, lab #1 review	2
2	9/9	Counting in binary, Boolean algebra	2, 4
	9/11	Standard forms for binary functions	4
	9/13	Quiz 1 , Karnaugh maps, lab #2 review	4
3	9/16	Karnaugh maps	4
	9/18	Karnaugh maps	4
	9/20	Quiz 2 , all NAND and all NOR circuits, lab #3 review	4
4	9/23	Sequential circuits – latch	7
	9/25	Sequential circuit timing, standard form, flip-flop	7
	9/27	Quiz 3 , D flip-flops, registers, lab #4 review	7
5	9/30	Counters	7
	10/2	Edge triggering	7
	10/4	Quiz 4 , JK and T flip-flops, lab #5 review	7
6	10/7	State machines: concept	7, 8
	10/9	State machine design and timing	9
	10/11	Quiz 5 , state machine example, lab #6 review	9
7	10/14	No class (Columbus Day)	
	10/16	(Monday schedule) State machine example	
	10/18	Exam review	
8	10/21	Midterm Exam (check drop date)	
	10/23	MSI devices	5, 6
	10/25	MSI devices	5, 6
9	10/28	MSI in state machine design example	5, 6
	10/30	Quiz 6 , mnemonic K-map	
	11/1	Number systems, common formats	2
10	11/4	Addition circuits	5
	11/6	Quiz 7 , subtraction circuits, overflow	5
	11/8	2's complement, multiplication circuits	2, 5
11	11/11	No class (Veteran's Day)	
	11/13	Stop watch design example	
	11/15	Quiz 8 , introduction to memory circuits	10
12	11/18	Tri-states, memory configurations	10
	11/20	DRAM, error control	10, 2
	11/22	Quiz 9 , ROM, ROM implementation of combo logic	10
13	11/25	PALs, PLAs, and FPGAs	10
	11/27	Programmable device example	
	11/29	No class (Thanksgiving break)	
14	12/2	Quiz 10 , conclusions and review	
	12/4	ELE202 project presentations	
	12/6	ELE202 project presentations	
15	12/9	ELE202 project presentations	
16	12/???	Final exam – specific date and time to be announced	