Single Stage Bipolar Amplifier Topologies

ELE 338

University of Rhode Island, Kingston, RI 02881-0805, U.S.A.

There are 3 important single stage amplifier topologies using the bipolar transistor: the common emitter, the common collector (or emitter follower) and the common base, shown in figures 1 through 3.

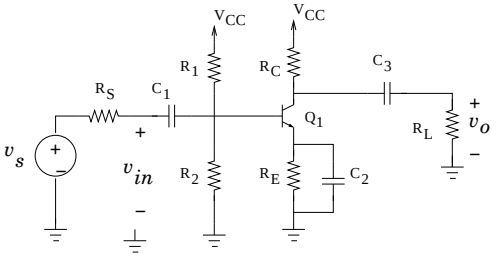

Figure 1. Common Emitter Amplifier.

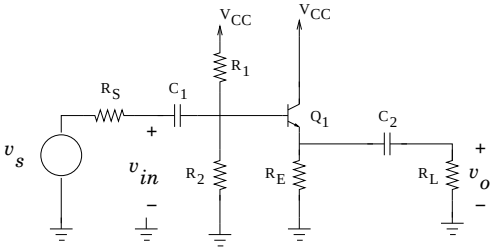

Figure 2. Common Collector Amplifier.

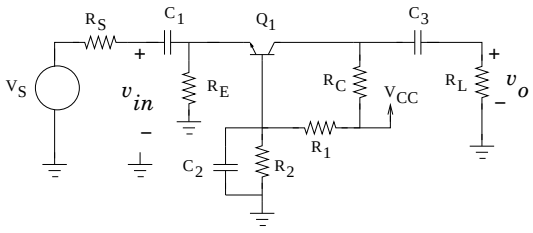

Figure 3. Common Base Amplifier.

[1] Tel: (401) 874-5482; fax: (401) 782-6422; e-mail: davis@ele.uri.edu

The design of any transistor amplifier starts with setting a stable DC operating point. The DC operating point of a bipolar transistor can be determined by finding two of the four parameters: $(I_C, I_B, V_{CE}, V_{BE})$. A stable DC operating point can be designed by biasing the transistor in such a way that the collector current, I_C, the base-emitter junction voltage V_{BE}, and the collector-emitter voltage, V_{CE} will be insensitive to variations in the DC current gain, β, and temperature, T.

Although the three amplifier topologies look different, the DC equivalent circuit is identical in all 3 cases (if we set $R_C = 0$ for the common collector). The DC equivalent circuit, assuming that the *npn* transistor is biased in the forward active mode (e.g. active mode), is shown in figure 4. The capacitors in each of the amplifier topologies are open circuits at DC, thus the circuit elements coupled to the amplifier core with series connected capacitors can be ignored for the DC analysis.

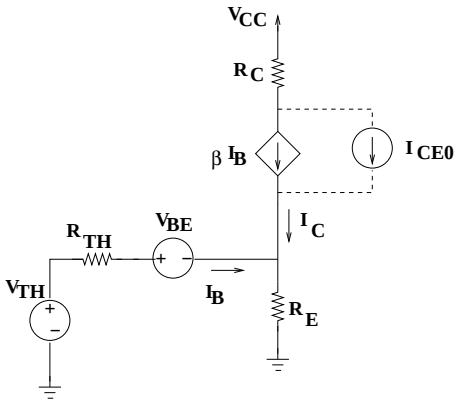

Figure 4. DC equivalent circuit suitable for simple *npn*-bipolar amplifier topologies.

The parameters are: $R_{TH} = R_1 \| R_2$, $V_{TH} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right)$ and $I_C = \beta I_B + I_{CE0}$. It is common for the β term to vary over a large portion of the range: 100 to $1,000$ for typical bipolar transistors. In order to maintain a stable operating point we will need a biasing scheme which will make I_C insensitive to variations in β.

There are two KVL relations given by

$$V_{TH} = I_B R_{TH} + V_{BE} + I_B(1+\beta)R_E \tag{1}$$

and

$$V_{CC} = I_C R_C + V_{CE} + I_B(1+\beta)R_E \tag{2}$$

If we substitute $I_C = \beta I_B + I_{CE0}$ into equation (1), and solve for I_C, we find

$$I_C = \frac{\beta\left(V_{TH} - V_{BE}\right)}{(\beta+1)\,R_E + R_{TH}} + \frac{R_E + R_{TH}}{(\beta+1)\,R_E + R_{TH}} I_{CE0} \tag{3}$$

Notice that the expression for $I_C = \beta I_B + I_{CE0}$ contains an independent current source, I_{CE0}, shown in figure 4, which is defined as the collector current when the base current is zero. This term represents the leakage current across the base-collector junction. For most applications of Silicon transistors, this term can be ignored (e.g. $I_C = \beta I_B$), yielding

$$\boxed{I_C = \frac{\beta\,(V_{TH} - V_{BE})}{(\beta + 1)\,R_E + R_{TH}}} \tag{4}$$

If $(\beta + 1)\,R_E \gg R_{TH}$, then

$$I_C \approx \frac{\beta}{(\beta + 1)} \frac{(V_{TH} - V_{BE})}{R_E} = \alpha \frac{(V_{TH} - V_{BE})}{R_E} \tag{5}$$

The term $\alpha = \frac{\beta}{\beta+1}$, remains very close to unity even for large variations in β. Thus, setting $(\beta + 1)\,R_E \gg R_{TH}$ guarantees minimal change in the DC operating point.

The second KVL expression given by equation (2) can be used to find the parameter V_{CE} and is given by

$$\boxed{V_{CE} = V_{CC} - I_C R_C - I_C \left(1 + \frac{1}{\beta}\right) R_E} \tag{6}$$

Using this analysis, it is possible to formulate a design procedure which will yield a stable DC operating point. The steps are:

1) Select the collector current I_C. This will also determine V_{BE} and I_B.
2) Set $V_{CC} = (3 - 5) \times V_{CE}$.
3) Set V_{RE}, the voltage drop across the resistor, R_E, to be equal or just slightly lower than V_{CE}.
4) Set $I_{R_1} = (10 - 100) \times I_B$.

Once these parameters are set, each of the four resistor values, R_1, R_2, R_C and R_E can be found.

If we assume that the amplifiers in figures 1 through 3 operate at *mid-frequency*,

The bypass capacitor values are selected such that the impedance presented in the band of operation is negligible when compared to the resistor values. This

means that for the *mid-frequency* AC analysis, all of the bypass capacitors can be replaced by short circuits. Any DC voltage source will be set to zero (e.g. *ac ground*); the supply voltages, for example, are shorted to AC ground.

The small signal equivalent circuit can be found for each topology by replacing the transistor with the AC equivalent (hybrid-π) model shown in figure 5. [2]

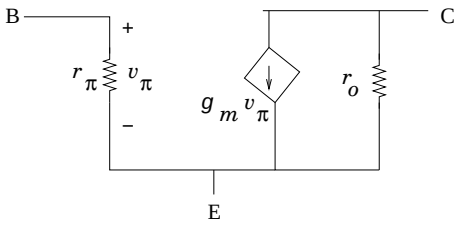

Figure 5. Small signal, hybrid-π model for the bipolar transistor.

Using these assumptions, the *mid-frequency*, AC equivalent circuit for each amplifier topology can be drawn. The *mid-frequency* small signal equivalent circuit for the common emitter, common collector and common base amplifier topologies are shown in figures 6 through 8.

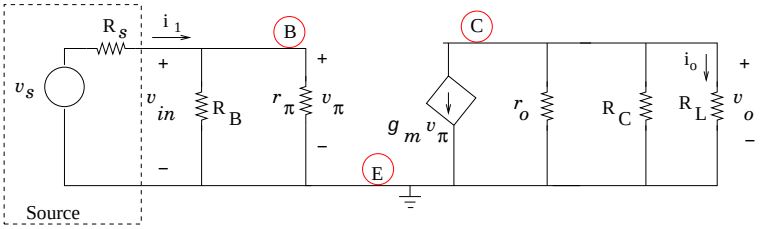

Figure 6. Common Emitter Amplifier small signal equivalent circuit.

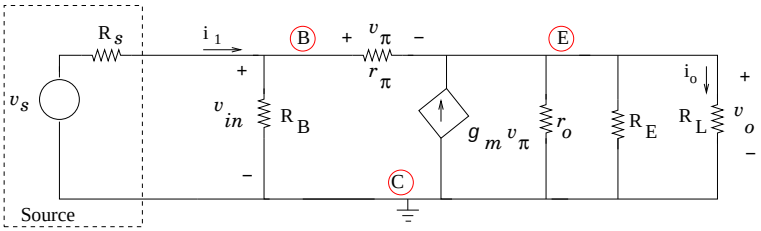

Figure 7. Common Collector Amplifier small signal equivalent circuit.

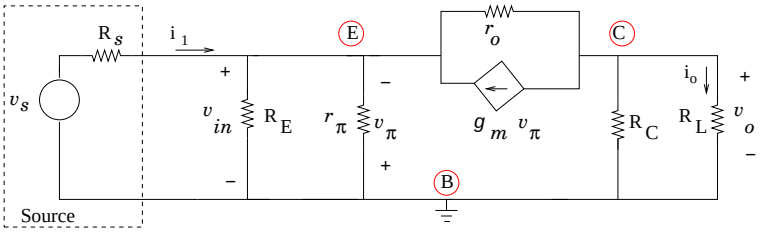

Figure 8. Common Base Amplifier small signal equivalent circuit.

[2] Note: The hybrid-π model is identical for the *npn* and *pnp* transistors.

The voltage and resistance of the signal source are given by v_S and R_S, respectively. The voltage and current at the input terminals of each amplifier topology are labeled v_{in} and i_1, respectively. The resistor, $R_B = R_{TH} = R_1 \| R_2$. The output voltage and current are labeled v_o and i_o, respectively. It is worth mentioning that an ideal, independent DC current source is replaced by an open circuit for the ac analysis; if the current source is not ideal, then the current source resistance is kept in the ac equivalent circuit.

It is useful to note that all of the small signal equivalent circuit model parameters shown in figure 5 are determined from partial derivatives.

The transconductance, g_m, is given by

$$g_m = \frac{\partial}{\partial V_{BE}}[I_C] = \frac{\partial}{\partial V_{BE}}\left[I_S e^{\frac{V_{BE}}{V_T}}\right] = \frac{I_C}{V_T} \tag{7}$$

where I_C is the current set by the DC operating point, $V_T = \frac{kT}{q}$, T is the absolute temperature in Kelvin, $k = 1.38 \times 10^{-23}\left[\frac{V-C}{K}\right]$ and $q = 1.602 \times 10^{-19}C$. $V_T = 26mV$ at room temperature ($T = 300K$).

The small signal base-emitter resistance, r_π, is defined as

$$r_\pi = \frac{\partial V_{BE}}{\partial I_B} \tag{8}$$

where V_{BE} and I_C are determined from the DC operating point.

The AC parameter, β, can be found from the relation

$$\beta = \frac{\partial I_C}{\partial I_B} = \left(\frac{\partial I_C}{\partial V_{BE}}\right)\left(\frac{\partial V_{BE}}{\partial I_B}\right) = g_m r_\pi \tag{9}$$

where g_m is the transconductance, r_π is the small signal base-emitter resistance and I_C, I_B and V_{BE} are determined from the DC operating point(for our purposes we have assumed that there is a single β parameter which is fine for exam 1).

The parameter r_o is given by

$$r_o = \left(\frac{\partial}{\partial V_{CE}}[I_C]\right)^{-1} \approx \frac{V_A}{I_C} \tag{10}$$

where V_A is the early voltage and I_C is the current set by the DC operating point.

Summarizing, to a *first order approximation*, we find:

$$\boxed{g_m = \frac{I_C}{V_T};\quad \beta = g_m r_\pi \quad \& \quad r_o \approx \frac{V_A}{I_C}} \tag{11}$$

where g_m, r_π & r_o are the small signal parameters, I_C is the current set by the DC operating point and V_A is the early voltage.

The small signal parameters for each amplifier topology are: the input impedance, Z_{in}, the voltage gain with respect to V_{in}, $A_{V_{in}}$, the voltage gain with respect to V_S, A_{V_s}, the current gain, A_I, the output impedance, Z_o and the power gain, A_p.

The small signal parameters have been summarized in Table 1 for the three amplifier topologies described in figures 6 through 8. Note that $r_o = \infty$ in the derivation of the common collector and the common base small signal parameters.

Topology Small Sig. Param.	Common Emitter	Common Collector	Common Base
Z_{in}	$r_\pi \| R_B$	$R_B \| \left[r_\pi + (1+\beta) R_E \| R_L\right]$	$R_E \| \left(\frac{r_\pi}{1+\beta}\right) \approx \frac{1}{g_m}$
$A_{V_{in}} = \frac{V_o}{V_{in}}$	$-g_m \left(r_o \| R_c \| R_L\right)$	$\frac{(1+\beta)R_E \| R_L}{r_\pi + (1+\beta)R_E \| R_L}$	$g_m R_C \| R_L$
$A_{V_s} = \frac{V_o}{V_s}$	$A_{V_{in}} \left(\frac{Z_{in}}{Z_{in}+R_S}\right)$	$A_{V_{in}} \left(\frac{Z_{in}}{Z_{in}+R_S}\right)$	$A_{V_{in}} \left(\frac{Z_{in}}{Z_{in}+R_S}\right)$
A_I	$A_{V_{in}} \frac{Z_{in}}{R_L}$	$A_{V_{in}} \frac{Z_{in}}{R_L}$	$A_{V_{in}} \frac{Z_{in}}{R_L}$
Z_o	$r_o \| R_C \approx R_C$	$\left[R_E \| \left(\frac{R_B \| R_S + r_\pi}{1+\beta}\right)\right] \approx \frac{1}{g_m}$	R_C
A_p	$\lvert A_{V_{in}} \rvert^2 \frac{Z_{in}}{R_L}$	$\lvert A_{V_{in}} \rvert^2 \frac{Z_{in}}{R_L}$	$\lvert A_{V_{in}} \rvert^2 \frac{Z_{in}}{R_L}$

Table 1
Summary of parameters for each amplifier topology.

A good designer must always be aware of the limitations of the circuit models used. It is worth noting that the small signal model is an approximation to a linear circuit. It is a very good approximation to the actual circuit behavior for low voltage swings in the common-emitter amplifier, for example; however, if the output voltage swing becomes too high, the values of the non-linear terms in the Taylor Approximation used for g_m will no longer be negligible (because $i_C = I_C + i_c \approx I_C$ will no longer hold and g_m will change with v_{in} causing the voltage gain to change as a function of v_{in}). Thus, the amplifier gain will vary with the input signal instead of remaining constant throughout the input signal swing. In the common-collector topology, the negative output voltage swing will will cause the transistor to go into cutoff if $\frac{-v_o}{R_L}$ is too large for a given I_C.

Other Single-Stage Bipolar Amplifier Topologies

This write up provides an introduction to the DC and AC analysis performed on simple, single-stage, bipolar amplifiers using the common four resistor biasing scheme. This is used often with single-ended supplies (e.g. positive voltage and ground). There is also the emitter-degenerated common emitter amplifier stage shown in figure 9. In this case the emitter bypass capacitor has been removed, thus the emitter will no longer be at ac ground for the mid-frequency, small signal analysis. There are also other DC biasing schemes which have not been mentioned. Namely, the self-biased approach can also be used for a single-ended power supply. If there is a dual power supply, that is one with a positive and negative supply rail (e.g. $\pm 15V$, then there is also a simple resistor biasing scheme. These are shown for the common-emitter amplifier in figures 11 and 12. A discussion of the different DC bias approaches would not be complete without mentioning current source biasing. A simple example is shown in figure 10 using a non-ideal current source attached at the emitter terminal. I_2 is the DC current source and R_2 is the resistance (or output impedance) of the current source. Only R_2 stays in the small signal model. Thus, R_E used in the resistor biasing shown in figure 9 will be replaced by R_2 in the small signal model when using the biasing approach shown in figure 10.

Finally, this has been done for the *npn* transistor; the analysis for the *pnp* transistor is quite similar.

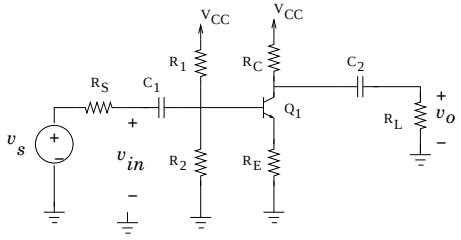

Figure 9. Emitter-degenerated, Common Emitter Amplifier.

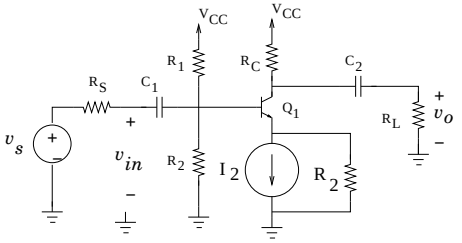

Figure 10. Common Emitter Amplifier biased with a non-ideal current source.

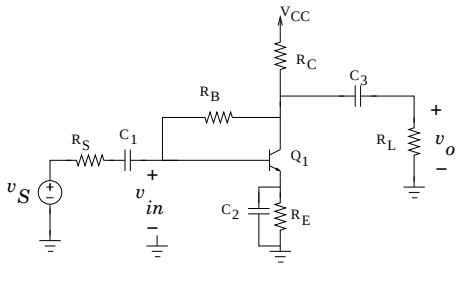

Figure 11. Self-biased Common Emitter Amplifier.

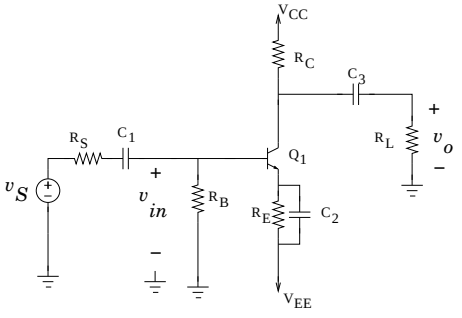

Figure 12. Common Emitter Amplifier biased with dual power supplies.