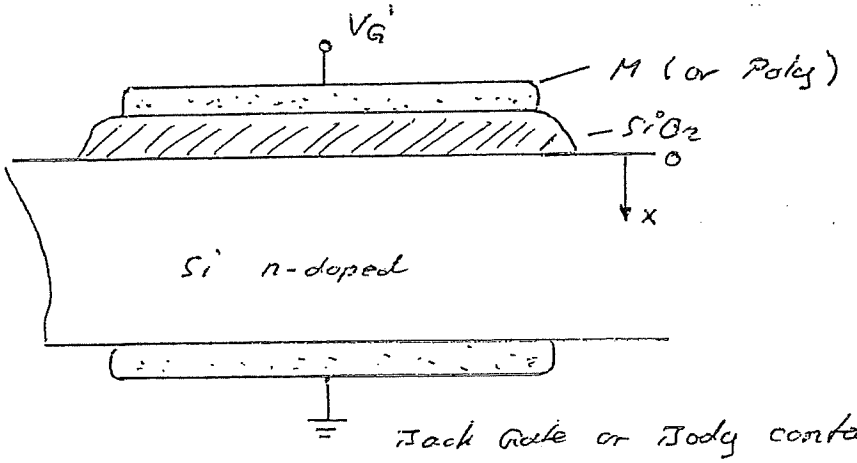
VI MOSFET Device Characteristics

1. The MOS Capacitor



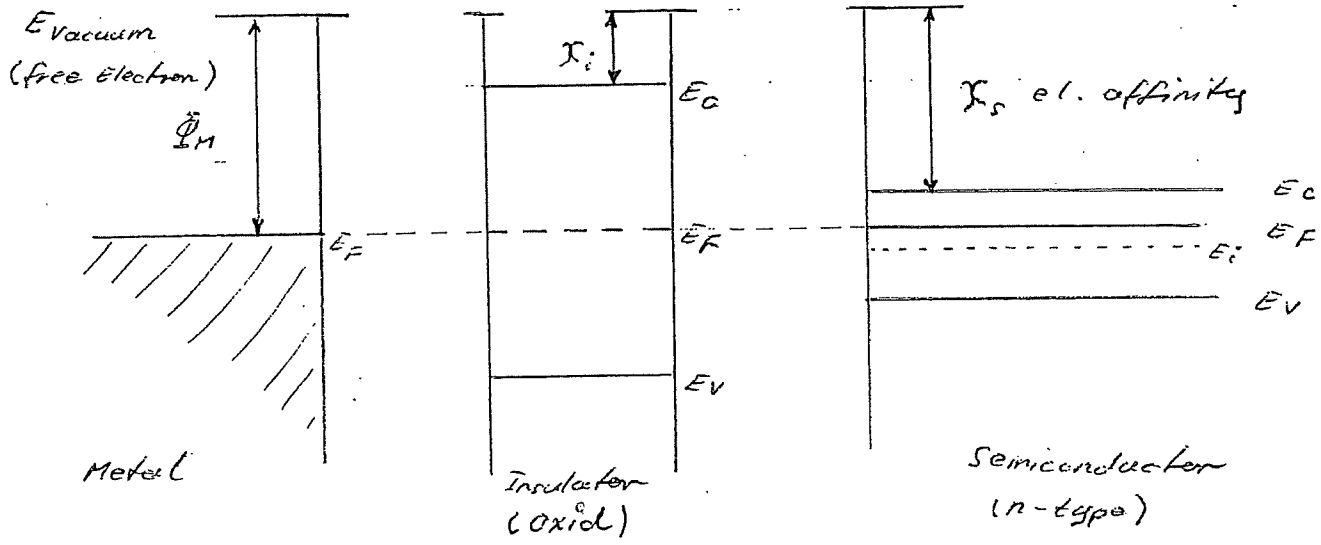
assumptions:

1. Gate is equipotential region
2. Oxide is perfect insulator
3. No charge centers in oxide
4. semiconductor is uniformly doped
5. Semic. is sufficiently thick so that a field-free region is formed before reaching the back contact
6. Back contact is ohmic
7. Capacitor is a one-dimensional structure in x
8. $\Phi_M = \chi_s + (E_C - E_F)$

Work fct. of Metal — el. affinity

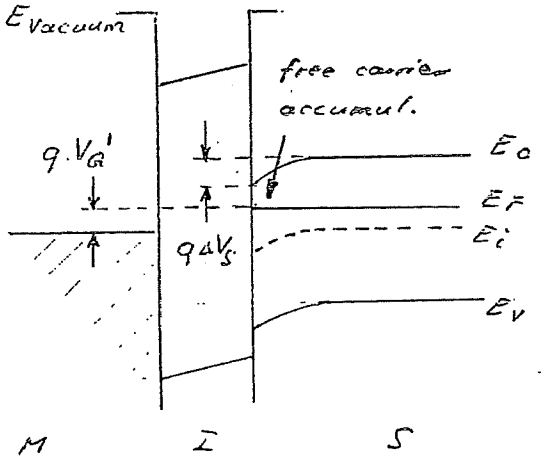
Energy Band Diagrams

zero Bias ($V_G' = 0$)



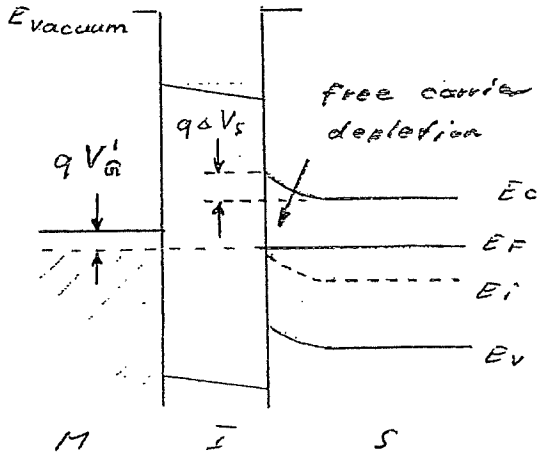
Nonzero Bias

a) $V_G' > 0$



ΔV_s: semiconductor surface potential

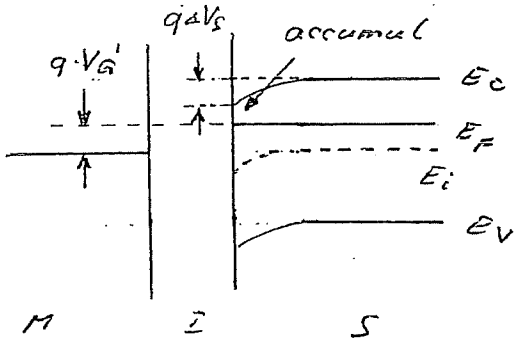
b) $V_G' < 0$ but $q\Delta V_s < (E_F - E_{i\infty})$

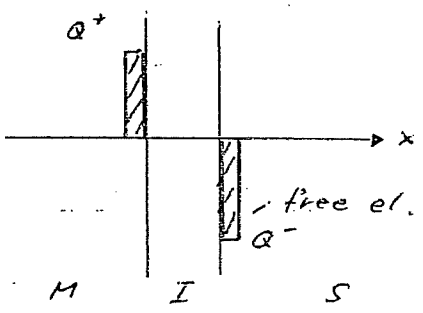


$E_{i\infty}$ denotes intrinsic Fermi level in field-free (bulk) Si

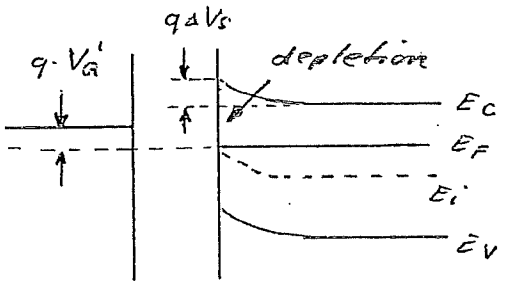
Charge Distribution for different Bias Voltages

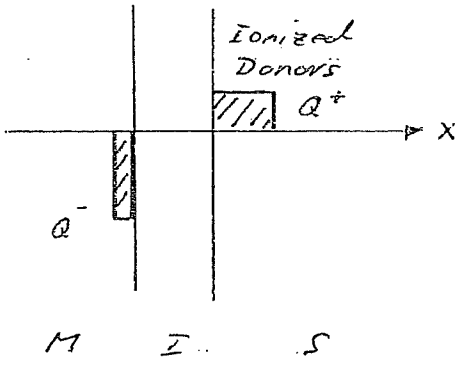
a) $V_G' > 0$



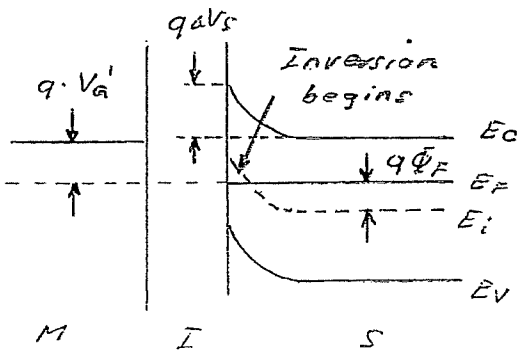


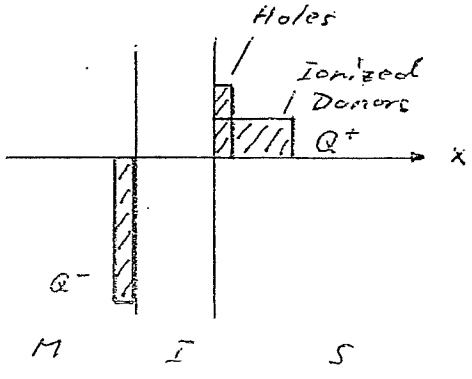
b) $V_G' < 0$ but $q\Delta V_S < (E_F - E_{i\infty})$





c) $V_G' < 0$ but $q\Delta V_S > (E_F - E_{i\infty})$





Inversion is achieved if

$$E_i(\text{surface}) - E_{i\infty} \geq 2(E_F - E_{i\infty}) \quad \text{or} \quad -q\Delta V_s \geq 2(E_F - E_{i\infty}) \qquad \text{Inversion } (n\text{-type } S)$$

The gate voltage V_G' that must be applied to achieve inversion is called Threshold voltage V_T'. Since $V_G' = \Delta V_{ox} + \Delta V_s$, we obtain:

$$V_T' = -2\frac{(E_F - E_{i\infty})}{q} + \Delta V_{ox} = +2\Phi_F + \Delta V_{ox} \qquad (n\text{-type } S)$$

Under inversion ($V_G' = V_T'$), the hole concentration at the surface of the semiconductor is equal to the donor concentration N_D (Definition). Hence

$$p_s = N_D = n_i\, e^{\frac{(E_F - E_{i\infty})}{kT}} = n_i\, e^{-\frac{\Phi_F q}{kT}}$$

$$W_T = \sqrt{\frac{2\varepsilon_s 2\Phi_F}{qN_D}}$$

and $$\Delta V_{ox} = -\frac{Q_{dep}}{C_{ox}} = -\frac{q \cdot N_D \cdot W_T}{C_{ox}} \qquad \left(C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}\right)$$

Solving for Φ_F and V_T' yields:

$$\Phi_F = -\frac{kT}{q} \ln\left[\frac{N_D}{n_i}\right] \qquad (p\text{-type } S)$$

$$V_T' = +2\Phi_F - \frac{q \cdot N_D W_T}{C_{ox}} \qquad p\text{-channel device}$$

In analogy to this result, we obtain for a p-doped semicond.

$$\Phi_F = +\frac{kT}{q} \ln\left[\frac{N_A}{n_i}\right] \qquad (p\text{-type } S)$$

$$V_T' = +2\Phi_F + \frac{q N_A W_T}{C_{ox}} \qquad n\text{-channel device}$$

Charge Density Distribution in MOS Capacitor

The exact solution of the charge density distribution inside the semiconductor is obtained by solving Poisson's eq.....

$$\left| \frac{dE}{dx} = \frac{\rho}{\varepsilon} \right|$$

where $\rho = q\,(p(x) - n(x) + N_D - N_A)$

$$\left| \begin{aligned} p(x) &= n_i\, e^{\frac{(E_i(x) - E_F)}{kT}} \\ n(x) &= n_i\, e^{\frac{(E_F - E_i(x))}{kT}} \\ N_D - N_A &= n_i \left[e^{\frac{-q\Phi_F}{kT}} - e^{+\frac{q\Phi_F}{kT}} \right] \end{aligned} \right|$$

Potential

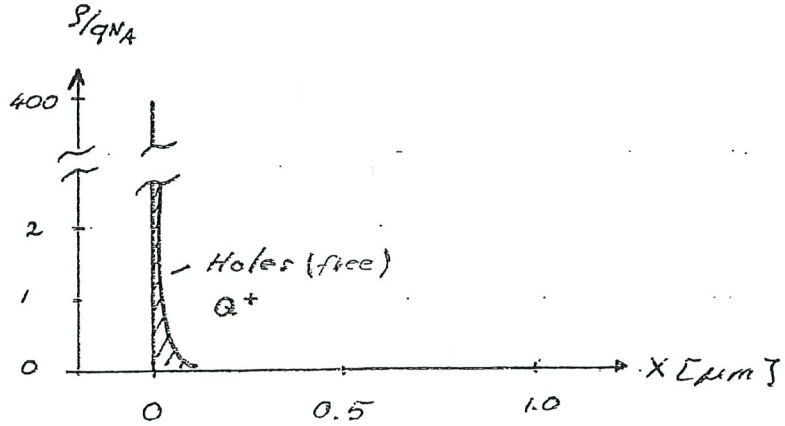
since $\rho = 0$ and $\Phi = 0$ in semiconductor bulk

Example: solution of Poisson's eq. for p-type Si with

$N_A = 10^{15}\,cm^{-3}$ $(\Phi_F = 0.3\,V)$

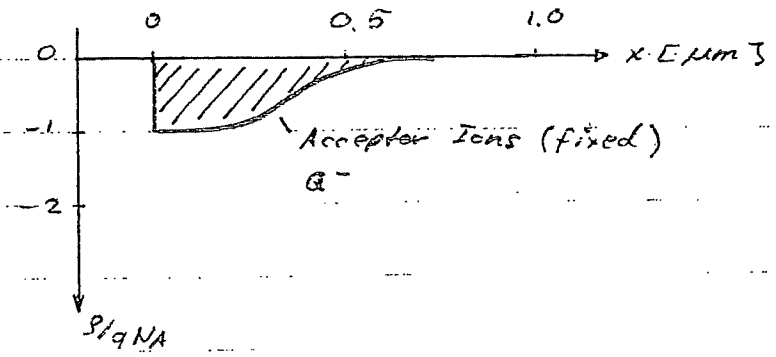
a) Accumulation

$\Delta V_S = -\frac{1}{2}\Phi_F$



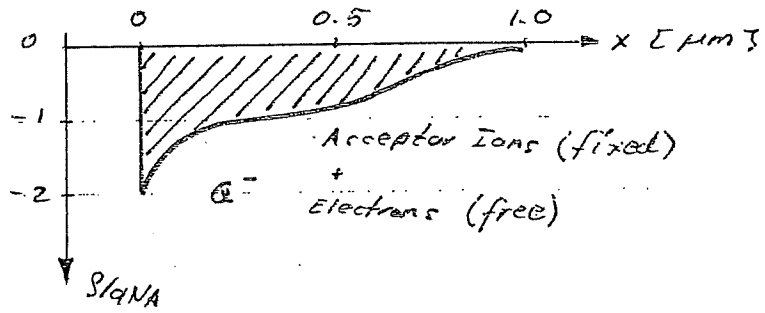
b) Depletion

$\Delta V_S = \Phi_F$



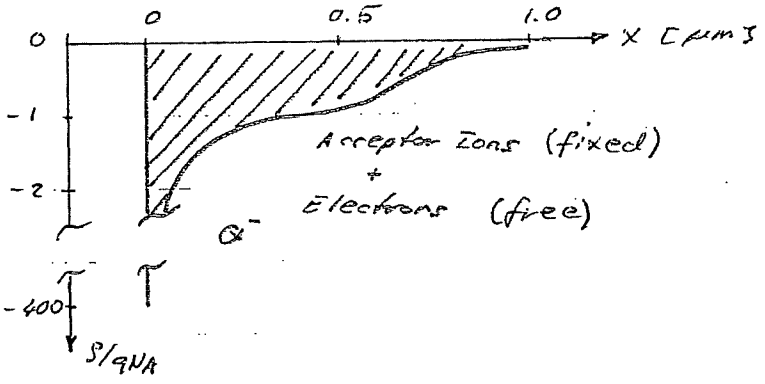
c) Onset of Inversion

$\Delta V_S = 2\,\Phi_F$



d) Deep Inversion

$\Delta V_S = 2.5\,\Phi_F$



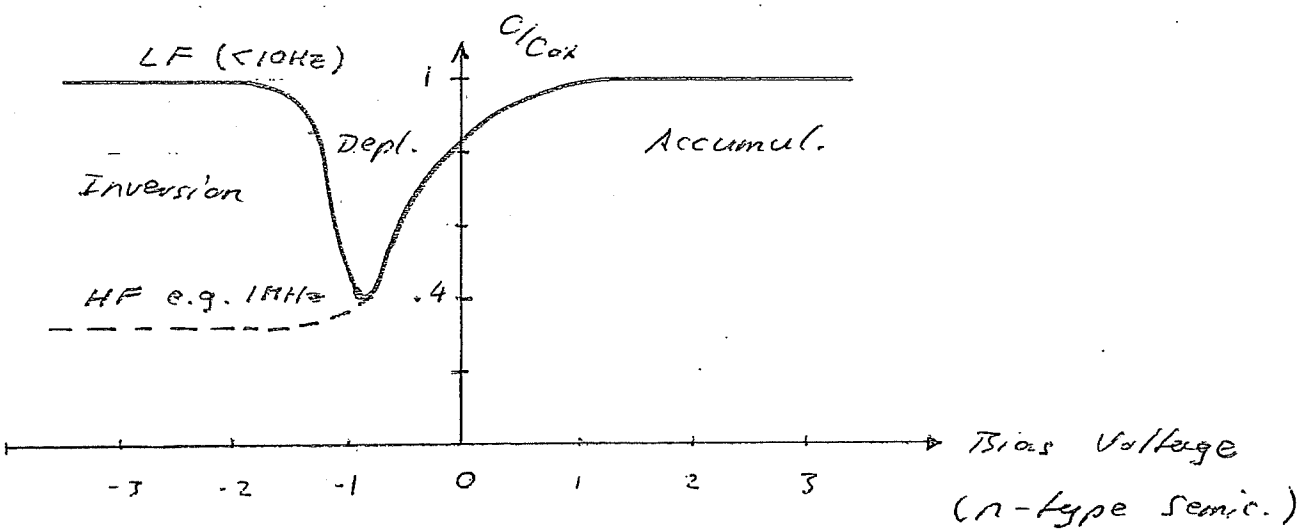
Note: The free charge carriers created through accumulation (holes in p-Si) or inversion (el in p-Si) reside in an extremely narrow portion of the semiconductor immediatly adjecent to the oxide layer. By comparison, the depletion portion (acceptor ions in p-Si) extends much deeper into the semiconductor.

The depletion width at the onset of inversion is approximately given by:

$$W_T = \sqrt{\frac{2\varepsilon_s 2\phi_F}{qN_A}} \qquad (p\text{-type})$$

Note that the depletion width approx. remains constant if the bias voltage is increased above the threshold voltage.

Capacitance - Voltage Characteristics



(n-type semic.)

Accumulation

$$C_{acc} \approx C_{ox} A_G = A_G \frac{\varepsilon_{ox}}{t_{ox}}$$

majority carrier

$\tau \approx 1ps$

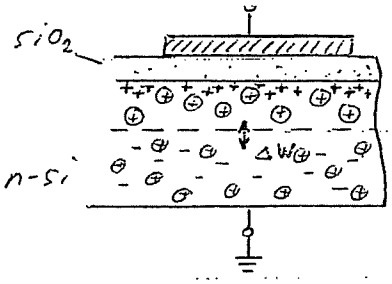
Notes $C_{ox} = \left[\frac{F}{m^2}\right]$

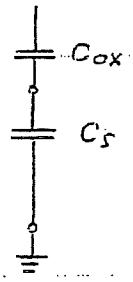
Depletion

$$C_{dep} \approx \frac{C_{ox} C_s}{C_{ox} + C_s}$$

ionized acceptors in depletion region

where $C_s = \varepsilon_s \frac{A_a}{W_T}$





$$C_{depl} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ox}}{\varepsilon_s}\frac{W_T}{t_{ox}}}$$

depl. width is changed by charging el. concentrated at the boundary between depl. region and the bulk semiconductor

→ involves majority carriers → short time const.

Inversion

In this case, charge variations in the semiconductor can be caused by small changes in the depletion width W (majority carriers + short time constant) or by changes in the inversion layer at the semiconductor - oxid interface (minority carriers must be generated → large time const.)

Thus, the effective capacitance under inversion depends on the frequency of the applied field

a) $\omega \to 0$

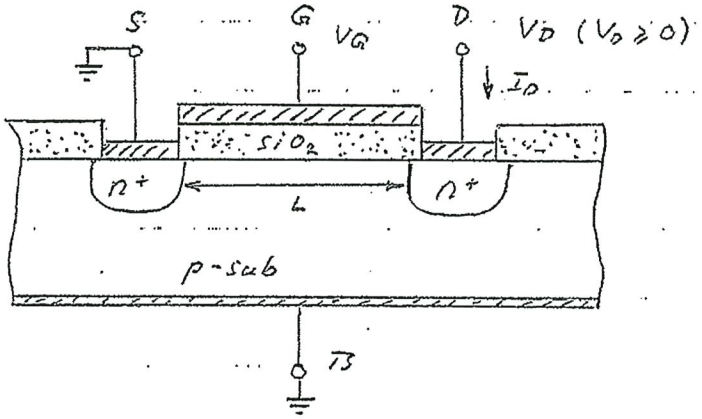
$$C_{inv} \approx C_{ox}$$

b) $\omega \to \infty$

$$C_{inv} \approx \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{depl}}} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ox}}{\varepsilon_s}\frac{W_T}{t_{ox}}}$$

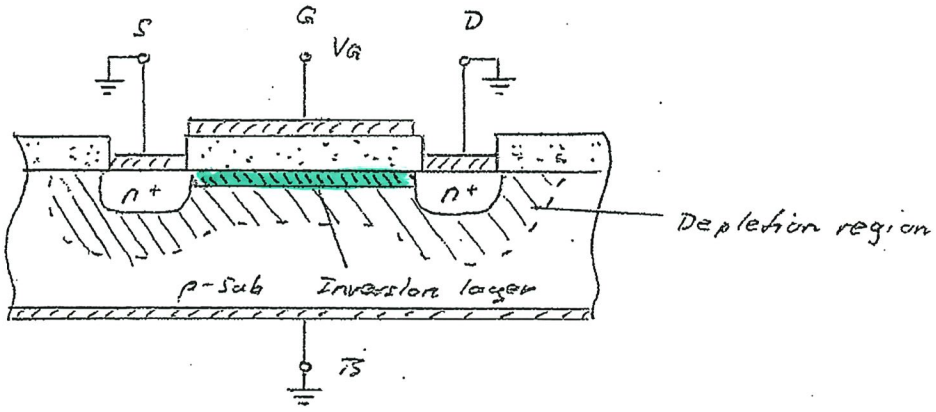
2. The MOS Fieldeffect Transistor

Basic Structure (n-channel)



Operation (enhancement-mode)

$V_G > V_T$ ($V_D = 0$)



Threshold voltage V_t : ($V_{SB} = 0$)

$$V_{t0} = V_{FB} + 2\phi_F + \frac{Q_{depl\,0}}{C_{ox}}$$ derived from MOS capacitor

where $V_{FB} = \phi_{MS} - \gamma_M \frac{Q_M}{C_{ox}} - \frac{Q_F}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}$ ($C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$)

and $Q_{depl_0} = q N_A W_T = \sqrt{2 \varepsilon_s q N_A 2\phi_F}$ ($\phi_F = \frac{kT}{q} \ln\left[\frac{N_A}{n_i}\right]$)

$V_{SB} \neq 0$ (Body - Effect)

$$V_t = V_{FB} + 2\phi_F + \frac{Q_{depl\,0} + Q_{depl} - Q_{depl\,0}}{C_{ox}}$$

$$= V_{t0} + \gamma \left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right]$$

$$= V_{t0} + \gamma \sqrt{2\phi_F} \left[\sqrt{1 + \frac{V_{SB}}{2\phi_F}} - 1\right]$$

where $\gamma = \frac{\sqrt{2 \varepsilon_s q N_A}}{C_{ox}}$ Body effect increases with $\sqrt{N_A} \cdot \frac{t_{ox}}{\varepsilon_{ox}}$

and $V_{t0} = V_{FB} + 2\phi_F + \gamma \sqrt{2\phi_F} = V_{FB} + \sqrt{2\phi_F} \left[\sqrt{2\phi_F} + \gamma\right]$

Example $N_A = 5 \cdot 10^{22}\ m^{-3}$

$V_{FB} = -0.6\,V$

$\phi_F = 0.4\,V$ $\Rightarrow$ $\gamma = 0.507\sqrt{V}$, $V_{t0} = 0.65\,V$

$\varepsilon_s = 10^{-10}\ \frac{As}{Vm}$

$C_{ox} = 2.5 \cdot 10^{-7}\ \frac{F}{m^2}$ $\therefore \gamma \cdot \sqrt{2\phi_F} = 0.45\,V$

$\therefore V_t(V_{SB}) = 0.65 + 0.45\left[\sqrt{1 + \frac{V_{SB}}{2\phi_0}} - 1\right]$

Quantitative Relationships

A) Square Law Theory (simple but not quite accurate)

current density in conducting channel:

$$J_y = q \mu_n n E_y = -q \mu_n n \frac{dV}{dy} \quad \text{(drift current)}$$

μ_n = electron mobility $\left[\frac{cm^2}{Vs}\right]$ $\left\{\mu = \frac{Vd}{E}\right\}$

Integrating the current density over cross sectional area of channel yields:

width W, depth X_0, channel width (z-direction)

$$I_D = \pm \int_0^W \int_0^{X_0} J_y \, dx \, dz = + W \int_0^{X_0} J_y \, dx$$

$$= \left(+ W \frac{dV}{dy}\right)\left(-q \int_0^{X_0} \mu_n n \, dx\right) = -W \frac{dV}{dy} \mu_n \int q n \, dx$$

$-\mu_n \cdot Q_N$; Q_N = mobile charge in channel if $V_a > V_T$ (inversion layer)

Since I_D is const. over full channel length, we can write:

$$\int_0^L I_D \, dy = I_D \cdot L = -W \mu_n \int_0^{V_D} Q_N \, dV$$

and finally

$$\boxed{I_D = -\mu_n \frac{W}{L} \int_0^{V_D} Q_N \, dV}$$

Calculation of channel charge Q_N:

assumption: charge added to the gate of an MOS-Cap is balanced by increases in the inversion layer charge ($V_{GS} \geq V_t$) — we assume $V_G = V_{ox} + 2\phi_F + V_{FB}$

Thus $Q_N = Q_G\big|_{V_{GS} \geq V_t} = Q_G\big|_{V_{GS} = V_t}$ ← onset of inversion

$$= C_{ox}(V_{GS} - 2\phi_F - V_{FB}) - C_{ox}(V_t - 2\phi_F - V_{FB})$$

($V_{GS} - 2\phi_F - V_{FB}$ = voltage between plates of Cox = V_{oxo})

$$\Rightarrow \underline{Q_N = -C_{ox}(V_{GS} - V_t)}$$

($= V_{oxo}$)

Finally, by replacing $(V_G - 2\phi_F - V_{FB})$ with $(V_{GS} - 2\phi_F - V_{FB} - V_t)$ where $0 \leq V \leq V_D$, we obtain

$$\underline{\underline{Q_N(y) = -C_{ox}[V_{GS} - V_t - V(y)]}} \quad (V_G \geq V_t)$$

and so

$$I_D = \mu_n \frac{W}{L} C_{ox} \int_0^{V_D} (V_{GS} - V_t - V)\, dV \quad (0 \leq V_D \leq V_{DS}, \; V_G \geq V_t)$$

$$= \mu_n \frac{W}{L} C_{ox}\left[(V_{GS} - V_t)\cdot V_D - \frac{1}{2}V_D^2\right]$$

/

pre-pinch-off characteristics

post-pinch-off characteristics:

$$I_D\Big|_{V_D > V_{Dsat}} = I_D\Big|_{V_D = V_{Dsat}} = I_{Dsat} \quad \text{(assumption: current remains constant)}$$

or

$$I_{Dsat} = \mu_n \frac{W}{L} C_{ox} \left[(V_{GS} - V_t) V_{Dsat} - \frac{1}{2} V_{Dsat}^2 \right]$$

Since $Q_N(L) = 0$ when $V_y(L) = V_{Dsat}$, we can write

$$Q_N(L) = -C_{ox} (V_{GS} - V_t - V_{Dsat}) = 0$$

$$\Rightarrow \underline{\underline{V_{Dsat} = [V_{GS} - V_t] = V_{eff}}}$$

$$\Rightarrow \boxed{I_D\Big|_{V_D \geq V_{Dsat}} = I_{Dsat} = \mu_n \frac{W}{L} C_{ox} \frac{1}{2} [V_{GS} - V_t]^2}$$

post-pinch-off characteristics

According to this eq., the saturation current varies as the square of the gate voltage above turn-on, the so called "square-law" dependence.

Channel Length Modulation

If $V_{DS} > V_{eff}$, the drain side of the conducting channel is pinched-off. The effective channel length is then given by

$$\left| L_{eff} = L - W_T(V_{DS}) \right| \quad \text{and} \quad \left| V_{eff} = (V_{GS} - V_t) \right|$$

where $$W_T(V_{DS}) = \sqrt{\frac{2\varepsilon_s\varepsilon_0(\phi_0 + V_{DS} - V_{eff})}{q N_{sub}}}$$

$$\frac{dI_D}{dV_{DS}} = \frac{dI_D}{dL_{eff}} \frac{dL_{eff}}{dV_{DS}} = -\frac{1}{2}\frac{W}{L_{eff}^2}\mu C_{ox} V_{eff}^2 \frac{dL_{eff}}{dV_{DS}}$$

$$\frac{dL_{eff}}{dV_{DS}} = -\frac{dW_T}{dV_{DS}} = -\sqrt{\frac{\varepsilon_s\varepsilon_0}{2q N_{sub}(\phi_0 + V_{DS} - V_{eff})}}$$

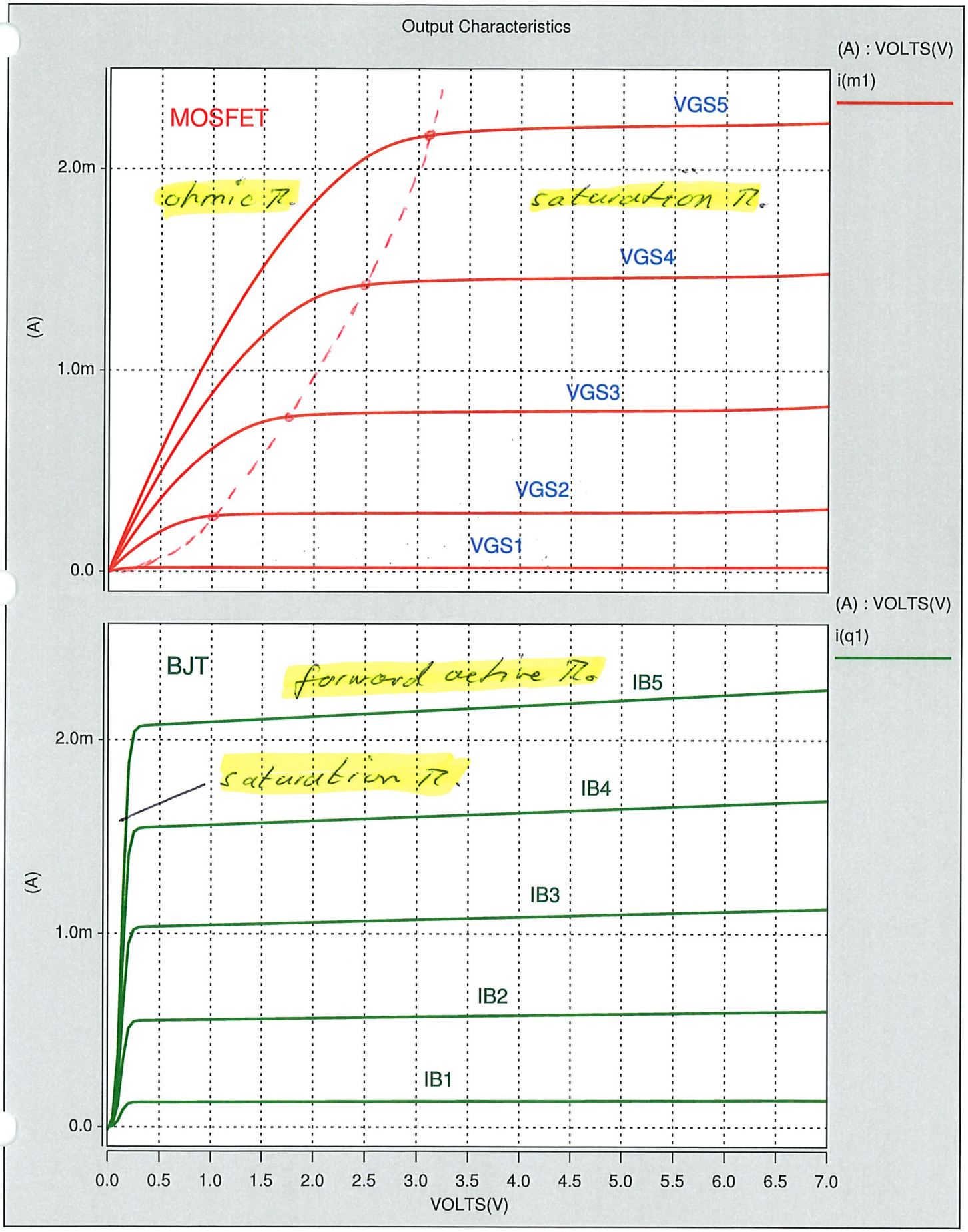
$$\therefore \frac{dI_D}{dV_{DS}} = \underbrace{\frac{1}{2}\frac{W}{L}\mu C_{ox} V_{eff}^2}_{I_{D0}} \cdot \frac{1}{L_{eff}} \sqrt{\frac{\varepsilon_s\varepsilon_0}{2q N_{sub}(\phi_0 + V_{DS} - V_{eff})}}$$

$$\therefore \left| I_D(V_{DS}) = I_{D0}\left(1 + \lambda[V_{DS} - V_{eff}]\right) \right|$$

where $$I_{D0} = \frac{1}{2}\frac{W}{L}\mu C_{ox} V_{eff}^2$$

$$\lambda = \frac{1}{L_{eff}} \sqrt{\frac{\varepsilon_s\varepsilon_0}{2q N_{sub}(\phi_0 + V_{DS} - V_{eff})}}$$

$$\left| I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L} V_{eff}^2 \left(1 + \lambda[V_{DS} - V_{eff}]\right) \right|$$


Output Characteristics
(A) : VOLTS(V)
i(m1)
MOSFET
ohmic R.
saturation R.
VGS5
VGS4
VGS3
VGS2
VGS1
2.0m
1.0m
0.0
(A)
(A) : VOLTS(V)
i(q1)
BJT
forward active R.
saturation R.
IB5
IB4
IB3
IB2
IB1
2.0m
1.0m
0.0
(A)
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0 6.5 7.0
VOLTS(V)

Summary MOSFET Equations

Threshold Voltage

n-ch. $$V_t = 2\Phi_F + \frac{1}{C_{ox}}\sqrt{4\varepsilon_s \Phi_p q N_{sub}} + V_{FB}$$

$$\Phi_p = \frac{kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right) \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

p-ch. $$V_t = -2\Phi_p - \frac{1}{C_{ox}}\sqrt{4\varepsilon_s \Phi_p q N_{sub}} + V_{FB}$$

Drain-Source Current (Square-Law Th.)

ohmic Region $V_{DS} \leq (V_{GS} - V_t)$

$$I_D = \frac{W}{L}\mu C_{ox}\int_0^{V_{DS}} (V_{GS} - V_t - V_x)\,dV_x$$

$$= \frac{W}{L}\mu C_{ox}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

saturation Region $V_{DS} > (V_{GS} - V_t)$

$$I_D = \frac{1}{2}\mu\frac{W}{L}C_{ox}\left[V_{GS} - V_t\right]^2 (1 + \lambda V_{DS})$$

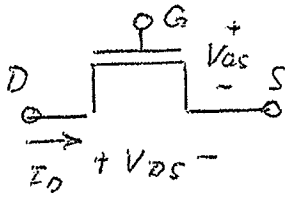
$$\lambda \cong \frac{1}{L}\sqrt{\frac{\varepsilon_s}{2qN_{sub}(\Phi_0 + V_{DS})}}$$ for $L > 1\mu m$

ch. length mod. factor

Si: $\varepsilon_s \cong 1.03 \times 10^{-10}\ \frac{As}{Vm}$ $\Phi_{0_{300k}} \cong 900\,mV$

MOSFET Operating Modes (N-Channel Dev.)

A) Cut-Off



$|V_{as} < V_t|$

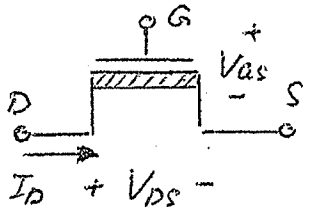
$\| I_D \cong 0 \|$

Model

open circuit

no channel formed

B) Triode or Ohmic Region

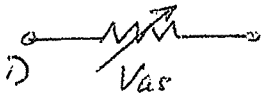


$|V_{as} \geq V_t \; ; \; V_{DS} < (V_{as} - V_t)|$

$\| I_D \cong \mu C_{ox} \frac{W}{L} [(V_{as} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2] \|$

Conductive channel between Drain-Source

Model



voltage controlled resistor

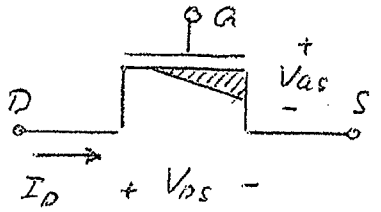
$\| g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{ox} \frac{W}{L} [V_{as} - V_t - V_{DS}] \|$

As long as V_{DS} is small with regard to $V_{as} - V_t$, the I/V characteristic of the MOSFET in the Triode region is approximately linear.

Example: $\mu C_{ox} \frac{W}{L} = 200 \, \mu A/V^2$ $\quad V_{as} - V_t = 2V$ $\quad V_{DS} = 0.1V$

$$\left| \begin{array}{l} g_{ds} \cong 400 \, \mu S \\ r_{ds} \cong 2.5 \, k\Omega \end{array} \right|$$

C) Forward active or Saturation Region



$$|V_{GS} \geq V_t \quad V_{DS} \geq (V_{GS} - V_t)|$$

$$V_{DS_{sat}} = (V_{GS} - V_t)$$

Channel is pinched-off at drain side of dep.

The depleted channel on the drain side creates a situation similar to a PN junction, where the free carriers can still cross the imposed barrier as long diffusion forces transport them to the very edge of the depletion region.

I/V Characteristic

$$\| I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [V_{GS} - V_t]^2 [1 + \lambda V_{DS}] \|$$

channel length Modul. factor

The I/V characteristic of a MOSFET in saturation is approximately parabolic.
If the MOSFET channel is comparatively short, the depletion region on the drain side shortens the ohmic region of the channel noticably, which in turn increases the current.

Note: $1/\lambda$ is the equivalent of the Early Voltage V_A in conjunction with BJTs.

Since the (drain) current of a MOSFET is essentially controlled by its Gate-Source voltage V_{GS}, we can think of the device acting like a voltage-controlled current source. We therefore introduce the transconductance g_m as follows:

$$\| g_m = \frac{\partial \bar{I}_D}{\partial V_{GS}} \cong \mu C_{ox} \frac{W}{L} [V_{GS} - V_t] \|$$

or

$$\| g_m = \frac{\partial \bar{I}_D}{\partial V_{GS}} = \sqrt{2 \bar{I}_{D sat} \mu C_{ox} \frac{W}{L}} \|$$

The dependance of the (saturation) current on the applied Drain-Source voltage V_{DS} can be described by the conductance g_{ds} defined as

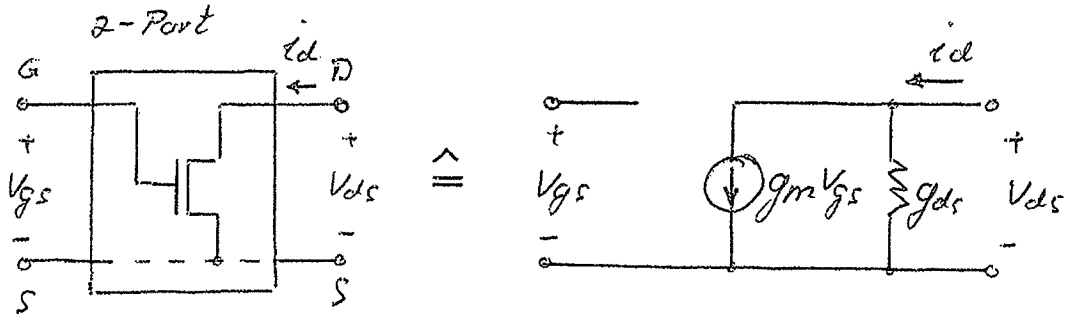
$$\| g_{ds} = \frac{\partial \bar{I}_D}{\partial V_{DS}} \cong \frac{1}{2} \mu C_{ox} \frac{W}{L} [V_{GS} - V_t]^2 \cdot \lambda \|$$

or

$$\| g_{ds} = \frac{\partial \bar{I}_D}{\partial V_{DS}} \cong \lambda \bar{I}_{D sat} \|$$

Due to the insulating layer between the gate and the channel, the Gate-Source and the Drain-Source junctions act like (ideal) capacitors.

The low frequency model of the MOSFET in saturation therefore looks like



Note The above model for the MOSFET (in common-source configuration) is a y-Parameter model with

$$\left|\begin{array}{ll} y_{11} \tilde{=} 0 & y_{21} = g_m \\ y_{12} \tilde{=} 0 & y_{22} = g_{ds} \end{array}\right| \qquad \begin{array}{l} g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_{DQ}} \\ g_{ds} = \lambda \cdot I_{DQ} \end{array}$$

Numerical Example:

Device Parameters: $\mu C_{ox} \frac{W}{L} = 200\,\mu A/V^2$

$\lambda = 0.05\ 1/V$

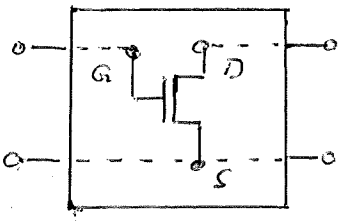
$V_t \tilde{=} 1\,V$

DC Biasing: $V_{GS} = 2V$

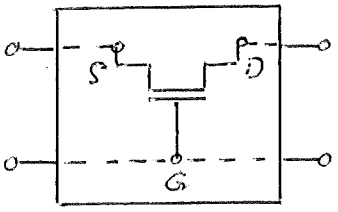
$V_{DS} = 2V$ $\quad \therefore V_{DS} > V_{GS} - V_t$

$$\left|\begin{array}{ll} I_{DQ} \tilde{=} 100\,\mu A & \text{saturation current} \\ g_m \tilde{=} 200\,\mu S & \text{transconductance} \\ g_{ds} \tilde{=} 10\,\mu S & \text{output conductance} \end{array}\right|$$

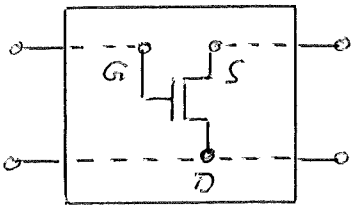
CS configuration



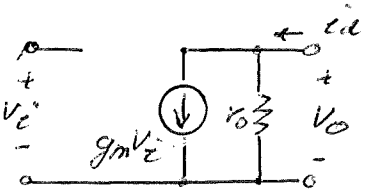
CG configuration

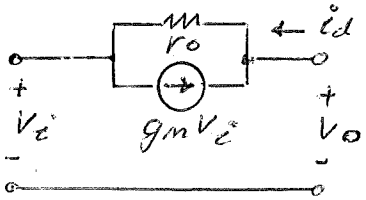


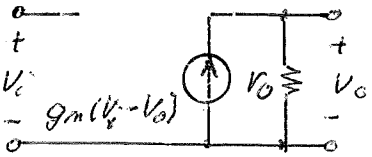
CD configuration



Small signal equivalent models





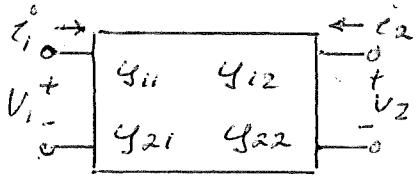


$$g_m = \sqrt{2 I_{DQ} k'} \qquad k = \mu C_{ox} \frac{W}{L}$$

$$r_o = \frac{1}{\lambda I_{DQ}}$$

Matrix Representation for 2-Port

Admittance Parameters (Y-Parameters)



$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left.\frac{i_1}{V_1}\right|_{V_2=0} \qquad y_{12} = \left.\frac{i_1}{V_2}\right|_{V_1=0}$$

$$y_{21} = \left.\frac{i_2}{V_1}\right|_{V_2=0} \qquad y_{22} = \left.\frac{i_2}{V_2}\right|_{V_1=0}$$

$$[Y_{CS}] = \begin{bmatrix} 0 & 0 \\ g_m & \frac{1}{r_o} \end{bmatrix} \qquad [Y_{CG}] = \begin{bmatrix} g_m + \frac{1}{r_o} & -\frac{1}{r_o} \\ -g_m - \frac{1}{r_o} & \frac{1}{r_o} \end{bmatrix} \qquad [Y_{CD}] = \begin{bmatrix} 0 & 0 \\ -g_m & g_m + \frac{1}{r_o} \end{bmatrix}$$

Complementary MOS enhancement Transistors

Planar CMOS Process

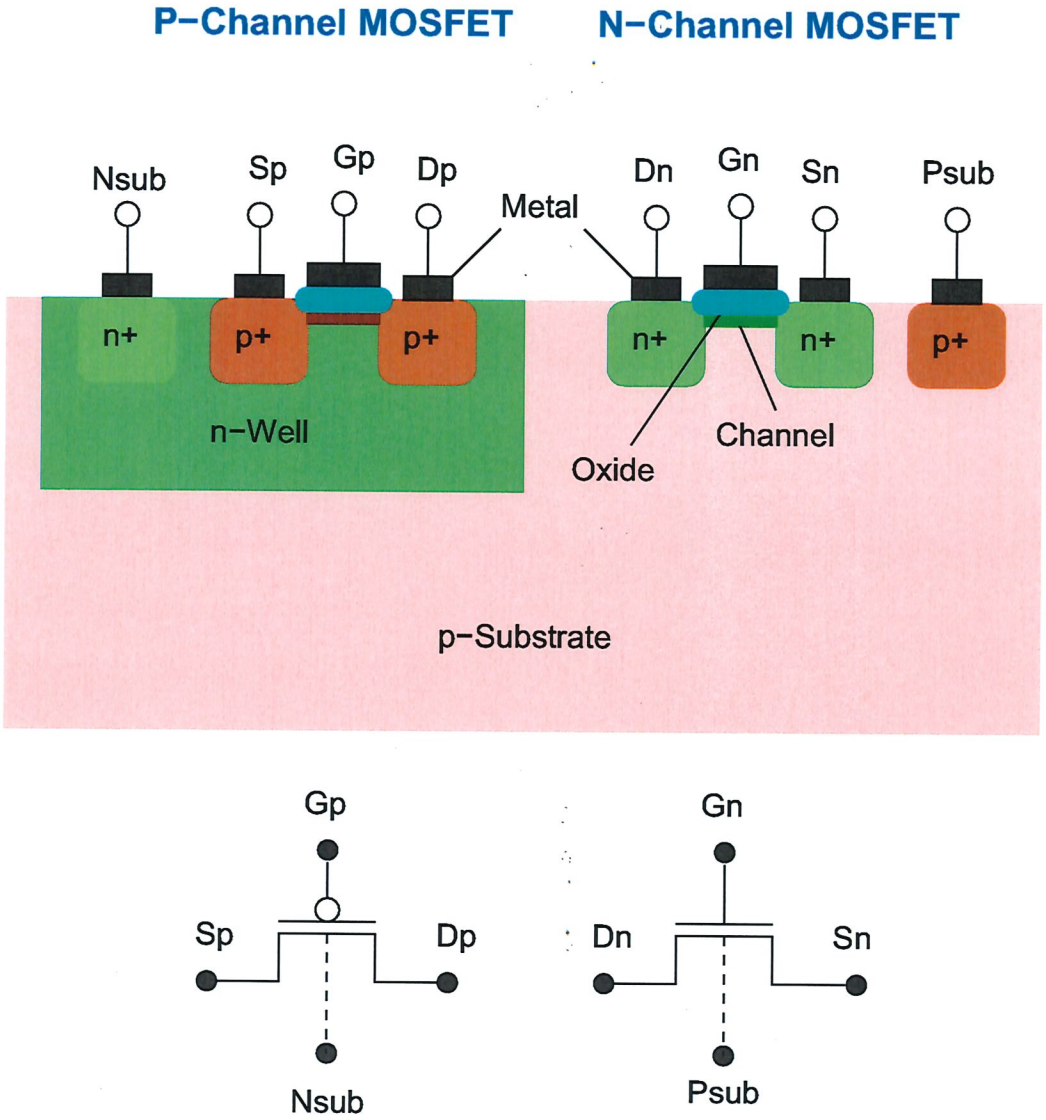
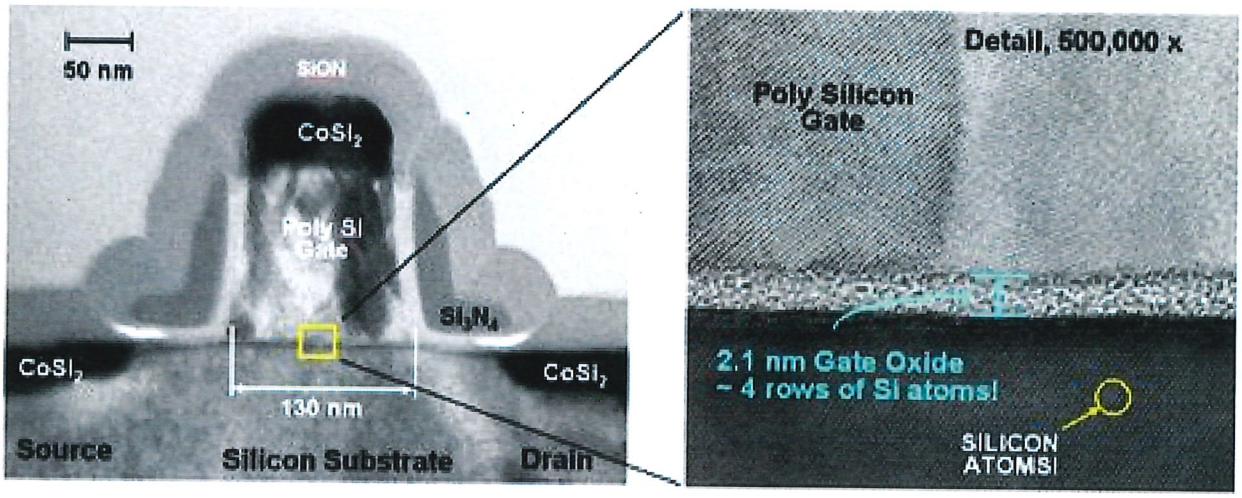


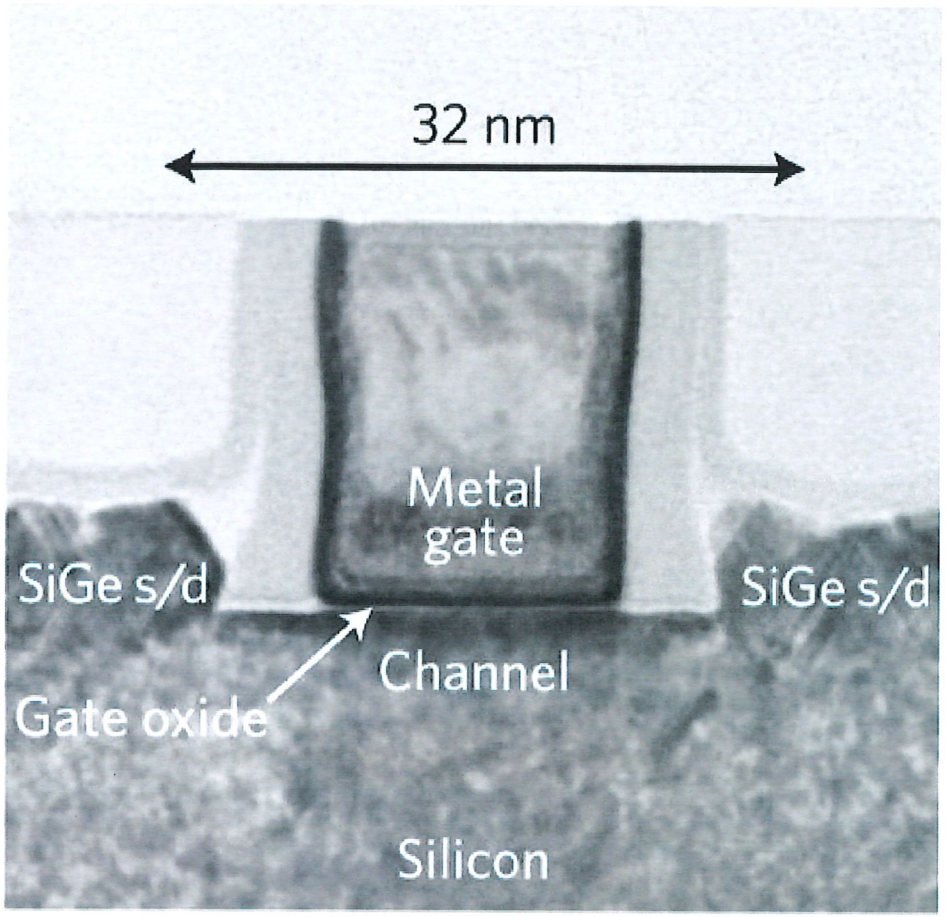
Figure 1 - Electron Micrograph of CMOS FET Cross Section



$CoSi_2$ Metal silicide with high conductivity

$t = 16\,nm$ $R_\square \approx 4\,\Omega$

MOSFET Cross Section



Metal Layers