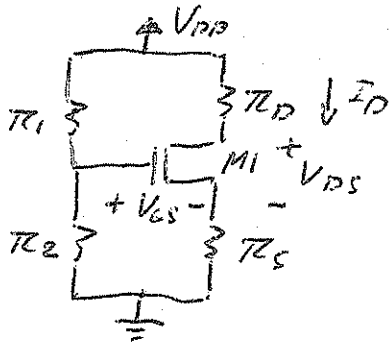
VII MOS Amplifiers

1. Biasing

A) Resistive Biasing



If M1 is in saturation, we can write

$$\boxed{I_D = k_n \cdot \frac{1}{2}\left[V_{GS} - V_{tn}\right]^2} \qquad k_n = \mu_n C_{ox}\left(\frac{W}{L}\right) \tag{1}$$

Furthermore

$$\boxed{I_D = \left[V_G - V_{GS}\right]\frac{1}{R_S}} \tag{2}$$

and

$$\boxed{V_G = V_{DD} \cdot \frac{R_2}{R_1 + R_2}} \tag{3}$$

Solving eq. (1) for V_{GS} yields

$$\boxed{V_{GS} = \sqrt{\frac{2 I_D}{k_n}} + V_{tn}} \tag{1'}$$

Finally, by inserting eq. (1') in (2), we obtain

$$\boxed{I_D = \left[V_G - V_{tn} - \sqrt{\frac{2 I_D}{k_n}}\right]\frac{1}{R_S}} \tag{4}$$

Solving eq. (4) for R_S yields:

$$\| R_S = (V_a - V_{tn}) \frac{1}{I_D} - \sqrt{\frac{2}{k_n I_D}} \| \qquad (5)$$

Using eq. (4) to calculate I_D requires solving a quadratic equation with the argument $\sqrt{I_D}$. The solution for $\sqrt{I_D}$ is:

$$\| \sqrt{I_D} = \frac{1}{\sqrt{2k_n}} \frac{1}{R_S} \left[\sqrt{1 + (V_G - V_{tn}) 2 k_n R_S} - 1 \right] \| \qquad (6)$$

or

$$\| I_D = \frac{1}{R_S} \left[V_G - V_{tn} + \frac{1}{k_n R_S} \left(1 - \sqrt{1 + (V_G - V_{tn}) 2 k_n R_S} \right) \right] \| \qquad (7)$$

The drain-source voltage can now be computed as

$$\| V_{DS} = V_{DD} - I_D (R_D + R_S) \| \qquad (8)$$

<u>Numerical Example</u>

$V_{DD} = 5V \quad V_{tn} = 0.7V \quad k_n = 200 \mu A/V^2$

$R_1 = 230 k\Omega \quad R_2 = 270 k\Omega \rightarrow | V_G = 2.7V |$

$R_D = 18 k\Omega \quad R_S = 10 k\Omega$

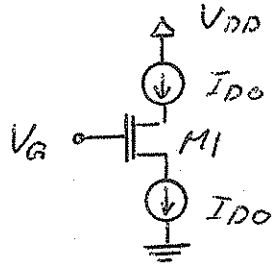
$$I_D = 10^{-4} \left[2 + \frac{1}{2} \left(1 - \sqrt{1 + 8} \right) \right] [A]$$

$$\| I_D = 100 \mu A \|$$
$$\| V_{DS} = 2.2 V \|$$

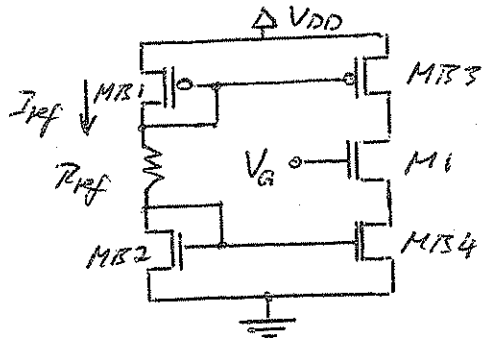
B) Biasing with current sources

Idea: By embedding the gain stage between 2 identical current sources, the gate voltage of the MOS amplifier becomes arbitrary (within practical limits).

Concept



Practical Implementation



The 2 current sources are realized by establishing a reference current in an additional branch and mirroring this current onto the gain stage (M1) by using 2 transistors (MB3 & MB4), which are identical to their counterparts (MB1 & MB2) in the reference branch.

→ Current Mirror

Note: This biasing method only establishes the dc drain current I_{DO} of the gain stage. The drain-source voltage will depend on the actual output resistors of the MOS

devices in the gain stage, i.e., r_{oM3}, r_{oM4} and r_{oM1}.

The reference current I_{ref} can be calculated as follows:

$$I_{ref} = \frac{1}{R_{ref}} \left[V_{DD} + V_{GSM3} - V_{GSM2} \right] \qquad (9)$$

where

$$V_{GSM1} = V_{tp} - \sqrt{\frac{2 I_{ref}}{k_p}} \qquad (10)$$

and

$$V_{GSM2} = V_{tn} + \sqrt{\frac{2 I_{ref}}{k_n}} \qquad (11)$$

Note: The threshold voltage V_{tp} of the p-channel device is negative!

Practically, eq. (9) is applied to solve for the reference resistor R_{ref}, since the designer selects the desired operating-point current I_{ref} with regard to the specific application.

Numerical Example

$V_{DD} = 5V$ $\quad V_{tn} = 0.7V$ $\quad V_{tp} = -0.7V$

$k_p = 200 \mu A/V^2$ $\quad k_n = 200 \mu A/V^2$

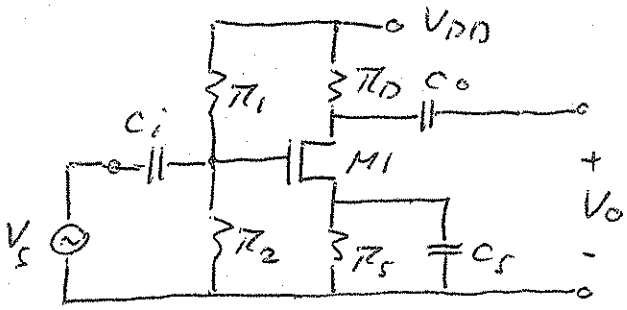
selected value: $I_{ref} = 100 \mu A$

$V_{GSM1} = -1.7V$; $\quad V_{GSM2} = +1.7V$; $\quad R_{ref} = 16 k\Omega$

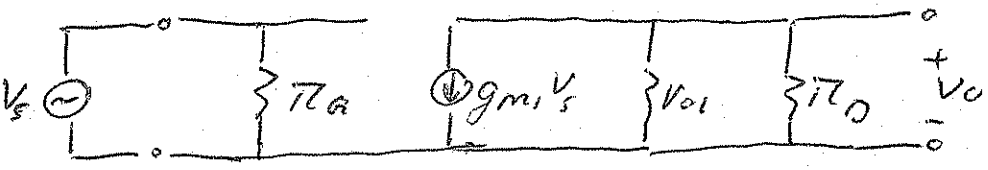
2. MOS Gain Stages

A) Common-Source (CS) Amplifier

2.1 CS Amplifier with resistive biasing circuit



AC equivalent circuit (caps act as AC shorts)



$$R_G = R_1 \parallel R_2 \qquad g_{m1} = \sqrt{2 I_{D1} k_1'}$$

$$r_{o1} = \frac{1}{\lambda_1 I_{D1}}$$

Input resistance: $R_{in} = R_G$

Output resistance: $R_{out} = r_{o1} \parallel R_D$

Voltage gain: $A_v = \frac{V_o}{V_i} = -g_{m1}\, r_{o1} \parallel R_D$

Numerical Example

$V_{DD} = 5V \quad V_{t1} = 0.7V \quad \mu_1 = 800 \mu A/V^2 \quad \lambda_1 = 0.025\ 1/V$

$R_1 = 280 k\Omega \quad R_2 = 220 k\Omega \quad R_D = 22 k\Omega \quad R_S = 10 k\Omega$

$\therefore \| I_{D1} = 100 \mu A \| \quad \| V_{DS} = 1.8V \| \quad V_{GS} = 1.2V$

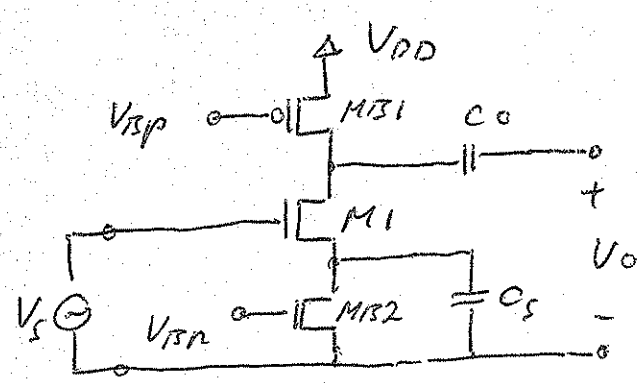
$$\left| \begin{array}{l} g_{m1} = 400 \mu S \\ r_{o1} = 400 k\Omega \\ R_G = 123.2 k\Omega \end{array} \right|$$

AC Performance

$$\left\| \begin{array}{l} R_{in} = 123.2 k\Omega \\ R_{out} = 20.85 k\Omega \\ A_V = -8.34 \end{array} \right\|$$

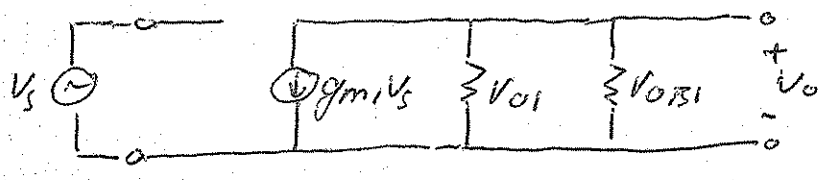
As demonstrated by this example, the CS amplifier using passive biasing yields relatively small voltage gain values. The gain could be increased slightly by increasing R_D (e.g. $R_D = 30 k\Omega$). Unfortunately, increasing R_D reduces the drain-source voltage (e.g. $R_D = 30 k\Omega \therefore V_{DS} = 1.0V$) and leaves little room for the output voltage swing. This dilemma can be overcome by employing an <u>active</u> biasing scheme.

2.2 CS Amplifier with current source biasing



Note: V_S must comprise a DC component sufficiently large to keep M1 in saturation

AC equivalent circuit (Caps act as AC shorts)



$$g_{m1} = \sqrt{2 I_{D1} k_1'}$$

$$r_{o1} = \frac{1}{\lambda_1 I_{D1}} \qquad r_{o3I} = \frac{1}{\lambda_{3I} I_{D1}}$$

Input resistance: $R_{in} = \infty$

Output resistance: $R_{out} = r_{o1} \parallel r_{o3I}$

Voltage gain: $A_V = \frac{V_o}{V_S} = -g_{m1} r_{o1} \parallel r_{o3I}$

or

$$A_V = -\sqrt{\frac{2k_1'}{I_{D1}}} \frac{1}{(\lambda_1 + \lambda_{3I})}$$

Numerical Example

$V_{DD} = 5V \quad V_{t1} = 0.7V \quad k_1 = 800\,\mu A/V^2$

$I_{D1} = 100\mu A \quad \lambda_1 = 0.025\,\frac{1}{V} \quad \lambda_{T1} = 0.025\,\frac{1}{V}$

$g_{m1} = 400\mu S$

$r_{o1} = 400k\Omega$

$r_{T1} = 400k\Omega$

$V_{GS1} = 1.2V$

If all 3 MOS transistors are well matched

$|V_{TS1} \approx 1.7V|$

AC Performance

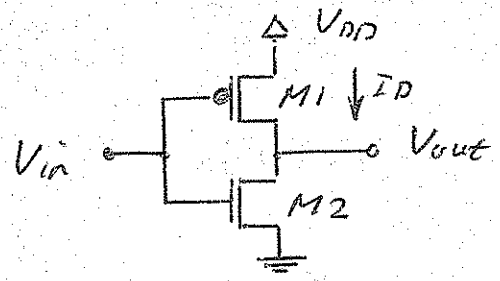
$r_{in} = \infty$

$r_{out} = 200k\Omega$

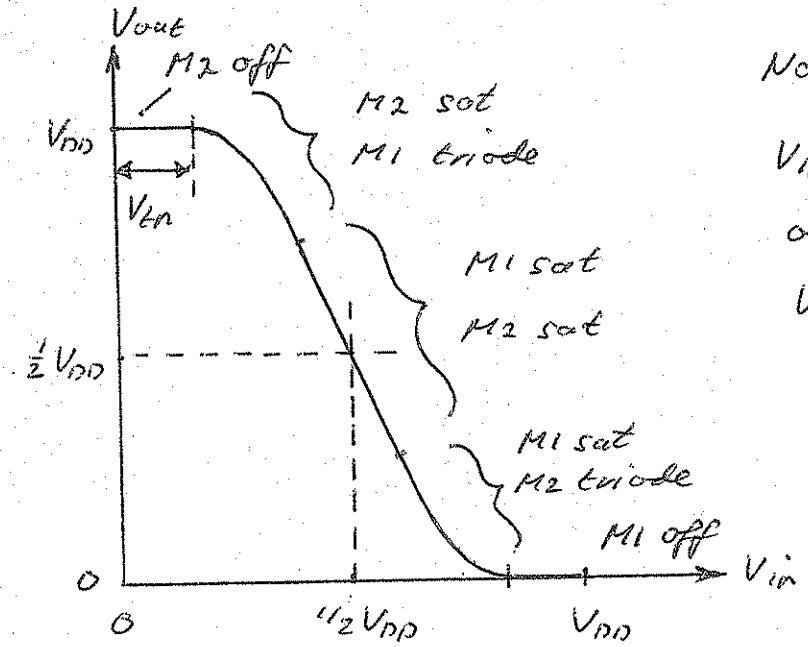
$A_V = -80$

Replacing the passive load resistor R_D by an MOS current source (→ active load) allows the designer to realize a much larger voltage gain without sacrificing output swing. The price for this improvement is the need for multiple biasing transistors. However, this has little practical significance on an integrated circuit (IC), since a transistor requires less (silicon) area than a (large) resistor.

Special Case: Self-biased CMOS Inverter



Large Signal Response

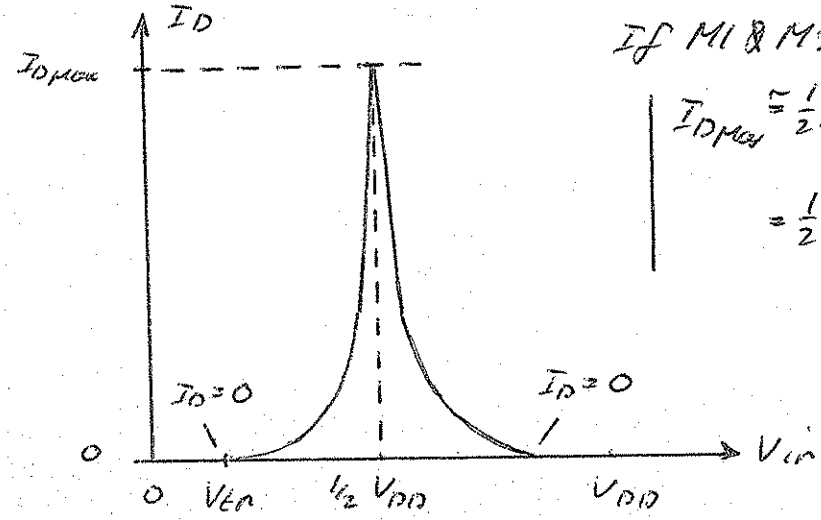


No current flows if

$V_{in} < V_{tn}$

or

$V_{in} > V_{DD} - |V_{tp}|$

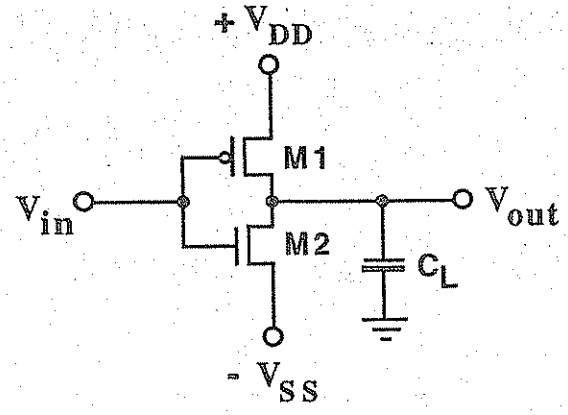


If M1 & M2 are well matched

$$I_{DMax} = \frac{1}{2}k_p\left[\frac{1}{2}V_{DD} - |V_{tp}|\right]^2$$

$$= \frac{1}{2}k_n\left[\frac{1}{2}V_{DD} - V_{tn}\right]^2$$

The self-biased CMOS Inverter



Linear gain

Assumption:

$$\frac{1}{2}\mu_1\left(\frac{W}{L}\right)_1 C_{ox} = \frac{1}{2}\mu_2\left(\frac{W}{L}\right)_2 C_{ox} = k \tag{1}$$

$$A_v \cong -\frac{4}{[V_{SS}-V_T][\lambda_1+\lambda_2]} \tag{2}$$

where

$$\lambda \cong \frac{1}{L_{eff}}\sqrt{\frac{\varepsilon_S}{2\,q\,N_{Sub}\,(\phi_B+V_{DS})}} \tag{3}$$

and

$$L_{eff} \cong L_{Drawn} - x_{LD} - \sqrt{\frac{2\,\varepsilon_S\,(\phi_B+V_{DS})}{q\,N_{Sub}}} \tag{4}$$

Therefore

$$A_v \propto L_{eff} \tag{5}$$

Settling behavior

A) Linear

$$V_{out}(t) = \Delta V\, A_v\,[1 - e^{-\frac{t}{\tau}}] \qquad t \geq 0 \quad \text{and} \quad \Delta V \leq \frac{V_T}{|A_v|} \tag{6}$$

where

$$\tau \equiv \frac{C_L}{k}\,\frac{1}{(\lambda_1+\lambda_2)\,[V_{SS}-V_T]^2} \tag{7}$$

Consequently

$$\tau \;\infty\; \frac{L_{eff}}{k} \;\infty\; L_{eff}\left(\frac{L}{W}\right) \tag{8}$$

B) Nonlinear

$$t_{settl.} \cong \frac{C_L}{k}\,\frac{2\sqrt{\Delta V(V_{SS}-V_T)} + (V_T-\Delta V)}{2\Delta V(V_{SS}-V_T)} \qquad \frac{V_T}{|A_v|} \leq \Delta V \leq V_T \tag{9}$$

$$t_{settl.} \cong \frac{C_L}{k}\,\frac{2\sqrt{\Delta V(V_{SS}-V_T)} - (\Delta V-V_T)}{2\,V_{SS}\,\Delta V - \frac{1}{2}(\Delta V+V_T)^2} \qquad V_T \leq \Delta V \leq (V_{SS}-V_T) \tag{10}$$

$$t_{settl.} \cong \frac{C_L}{k}\,\frac{1}{\frac{1}{2}V_{SS} + (\Delta V-V_T)} \qquad (V_{SS}-V_T) \leq \Delta V \leq V_{SS} \tag{11}$$

Numerical Example (90% settling times according to SPICE)

$V_{DD} = V_{SS} = 2.5V$
$V_T = 0.8V$
$C_L = 400fF$
$k = 100\mu A/V^2$

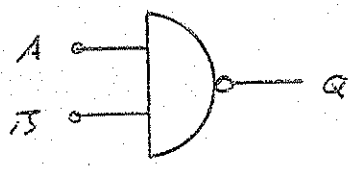
ΔV [V]	$t_{settl.}$ [ns]
0.2	10.4
0.3	7.6
0.4	6.0
0.6	4.4
0.9	3.1
1.2	2.5
1.6	2.0
2.0	1.6
2.5	1.4

Static CMOS Logic Gates

Consider MOS device as ideal switch

NAND

Symbol

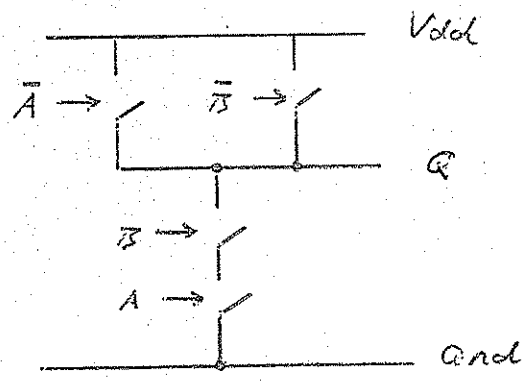


Truth table

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

$Q = \overline{A \cdot B}$

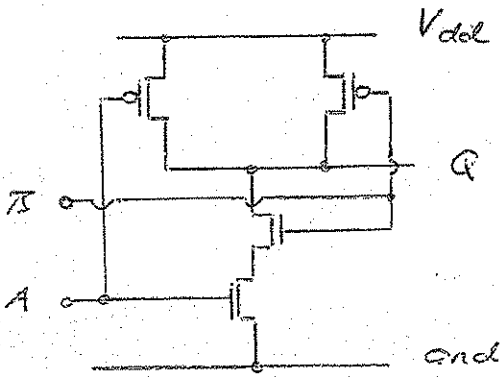
Implementation



where 

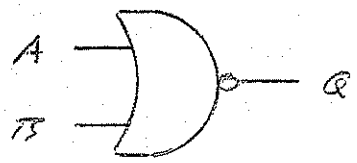
Switch which is closed while A is high

CMOS Circuit



NOR

Symbol

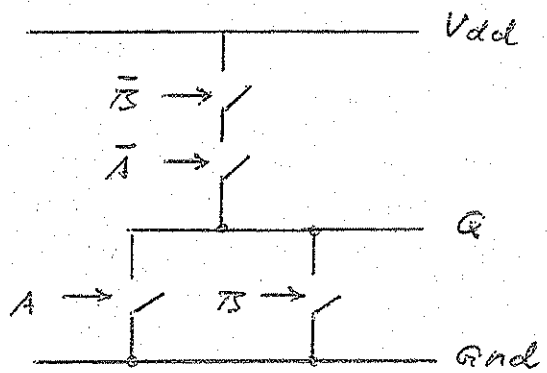


Truth Table

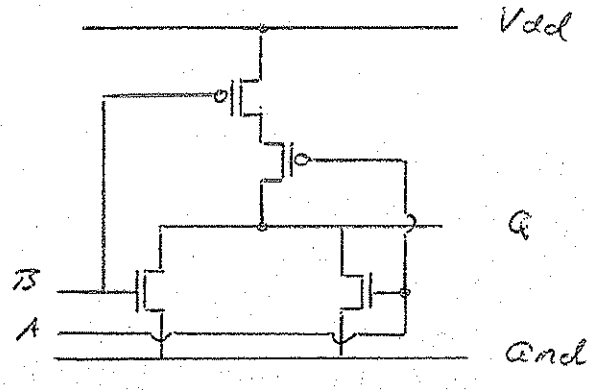
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

$Q = \overline{A + B}$

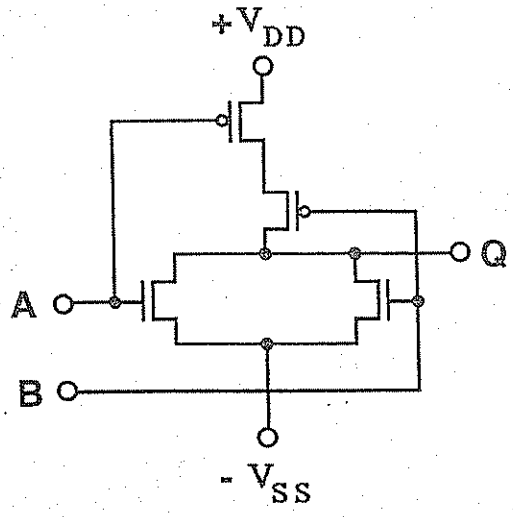
Implementation



CMOS Circuit



CMOS NOR Gate



CMOS NAND Gate