ELE 344 - LAB 1

COMMON-EMITTER AMPLIFIER

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Section 2

PURPOSE OF EXPERIMENT:

The purpose of the experiment is to be exposed to typical design problems with multiple degrees of freedom, where it is the job of the designer to find a compromise between sometimes conflicting performance requirements. In this case, the manipulation of a common-emitter amplifier's component values had to be manipulated to meet the requirements of each task.

EXPERIMENTAL PROCEDURES:

TASK 1:

ANALYSIS: Task 1 required consideration of the given circuit model, and the derivation of an expression for the bias current I_C, containing only R_1, R_2, R_{E1}, R_{E2}, V_{BE} and β. This required DC analysis, so the DC equivalent model had to be drawn. Then, from here, considering the Kirchhoff voltage loop formed between the upper rail voltage and ground, through R_1 and R_2, the expression could be derived.

DATA AND CALCULATION: The KVL equation is shown below.

$$V_{TH} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}, \qquad R_{TH} = R_1 \| R_2, \qquad R_E = R_{E1} + R_{E2}$$

$$V_{TH} = R_{TH} I_B + V_{BE} + R_E I_B (1 + \beta)$$

From this equation, the derivation was straightforward. The idea is to simply isolate Ic and use values which are either known or allowed to be included.

$$V_{TH} - V_{BE} = R_{TH} I_B + R_E I_B (1 + \beta)$$

$$V_{TH} - V_{BE} = R_{TH} \frac{I_C}{\beta} + R_E \frac{I_C}{\beta} (1 + \beta)$$

$$V_{TH} - V_{BE} = I_C \frac{R_{TH}}{\beta} + I_C R_E \left(\frac{1}{\beta} + 1\right)$$

$$V_{TH} - V_{BE} = I_C \left(\frac{R_{TH}}{\beta} + R_E \left(\frac{1}{\beta} + 1\right)\right)$$

$$I_C = \frac{V_{TH} - V_{BE}}{\frac{R_{TH}}{\beta} + R_E \left(\frac{1}{\beta} + 1\right)}$$

RESULTS: The resulting expression for I_C is shown above.

TASK 2:

ANALYSIS: Task 2 requires an analysis of the voltage gain at mid-band frequencies. This implies AC analysis. The small signal equivalent circuit was drawn and subsequently analyzed.

DATA AND CALCULATION: A few steps led to the voltage gain equation. First, V_{out} and V_{in} had to be calculated separately before their ratio could be found.

$$A_{Vin} = \frac{V_{out}}{V_{in}}, \qquad V_{out} = R_C \| R_L (-g_m V_\pi), \qquad V_{in} = V_\pi + V_\pi \left(g_m + \frac{1}{R_\pi} \right)$$

From here, putting V_{out} over V_{in} and making a few cancellations will result in the voltage gain equation in question.

$$A_{Vin} = \frac{V_{out}}{V_{in}} = \frac{-g_m R_C \| R_L}{\left(1 + g_m + \frac{1}{R_\pi}\right) R_{E1}}$$

$$A_{Vin} = \frac{-R_C \| R_L}{\frac{V_T}{I_C} + R_{E1}}$$

RESULTS: The resulting expression for the voltage gain of this common-emitter circuit is shown above. It is important to note that the value of R_{E1} should be considerably larger than the value of $1/g_m$ so that the gain is stable and controlled.

TASK 3:

ANALYSIS: Task 3 calls for an expression for the input impedance of the circuit, Z_{in}. This also requires AC analysis. First, the input resistance, not including the base resistors (R_1 and R_2). Then, the base resistors are included to complete the expression.

DATA AND CALCULATION: The input resistance without the base resistors is shown below. It was acquired by inspection of the small signal model.

$$r'_{in} = \frac{V_{in}}{i_b} = (1 + \beta) \frac{V_T}{I_C} + (1 + \beta) R_{E1}$$

From here, this needs to be put in parallel with the base resistors. This is shown below, and concludes the derivation.

$$Z_{in} = \frac{V_{in}}{i_{in}} = r'_{in} \| R_1 \| R_2$$

RESULTS: The resulting expression for the input resistance can be seen above. It is in a simplified form, making it easier to read.

TASK 4:

ANALYSIS: Task 3 is when the designing and choice-making must begin. Given the voltage swing must be at least 4V, one can derive a value for I_C based on R_C and the swing. With this value, and with the knowledge that when the rail voltage is above 5V, V_{CE} and V_{RE} are about equal, one can divide the remaining voltage from the upper rail between V_{CE} and V_{RE}, from which resistance can be calculated, since current values are known. With knowledge of these values, both R_{E1} and R_{E2} can be given initial estimates, which, combined with the restriction on Z_{in}, will lead to the calculation of R_1 and R_2.

DATA AND CALCULATION: First, IC must be selected according to the values given. Since the swing must be at least 4V, we have chosen 5V.

$$I_C = \frac{V_{swing}}{R_C} = \frac{5V}{3.9k\Omega} = \ 1.28mA$$

From here, this can be used in a rearranged gain equation, to estimate a value for R_{E1}.

$$R_{E1} = \frac{-R_C||R_L}{A_{Vin}} - \frac{V_T}{I_C} = \sim 120\Omega$$

Using another equation, one for V_{RE}, we can find the value of R_{E1} and R_{E2} in series, and, with a value for R_{E1}, we can determine R_{E2}. We have the value for V_{RE}, with the knowledge that when the rail voltage is above 5V, V_{CE} and V_{RE} are about equal.

$$V_{RE} = \frac{I_B + I_C}{R_E} \Rightarrow R_{E2} = \frac{I_B + I_C}{V_{RE}} - R_{E1} = 1.82k\Omega$$

Setting Z_{in} = 6kΩ, which is greater than 5kΩ, the restriction, one can finally determine values for R_1 and R_2. The following equations are solved for R_{TH} then for R1 and R2.

$$V_{TH} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

$$V_{TH} = R_{TH} I_B + V_{BE} + R_E I_B (1 + \beta)$$

$$If\ Z_{in} = \ 6k\Omega, \qquad R_1 = 25.7k\Omega, and\ R_2 = 12.4k\Omega$$

RESULTS: The following results were acquired from this section:

$$R_{E1} = \ 120\Omega$$

$$R_{E2} = \ 1.82k\Omega$$

$$If\ Z_{in} = 6k\Omega, \quad R_1 = 25.7k\Omega, and\ R_2 = 12.4k\Omega$$

These values will be close to those used in the practical circuit and the PSpice model. Not all of these resistor values are available, however, and will have to be substituted.

TASK 5:

ANALYSIS: In task 4, the transistor output resistance was neglected. Task 5 asks for justification for this decision. One can determine the impact of r_O by finding its value with an estimated early voltage, then comparing that value to R_C.

DATA AND CALCULATION: Assuming the early voltage was fairly reasonable, say 80V, one can calculate r_O to determine its impact on the circuit.

$$r_o = \frac{V_A}{I_C} = \frac{80V}{1.28mA} = \sim 80k\Omega$$

If r_O was put in parallel with R_C the way it would be in the circuit, we see immediately that it would only affect about a 5% change to the value of R_C.

RESULTS: Obviously, this justifies the removal of r_O; it's inclusion would only change the results by about +-5%.

TASK 6:

ANALYSIS: Given that the frequency is the inverse of the product of the resistance, capacitance, and a scaling factor (2π), we can calculate the capacitance based on the corner frequency of 100Hz. However, since it is desirable to have smaller capacitance values for C_O and C_I, we should evaluate these for 10Hz.

DATA AND CALCULATION: The following equations show the capacitance calculations.

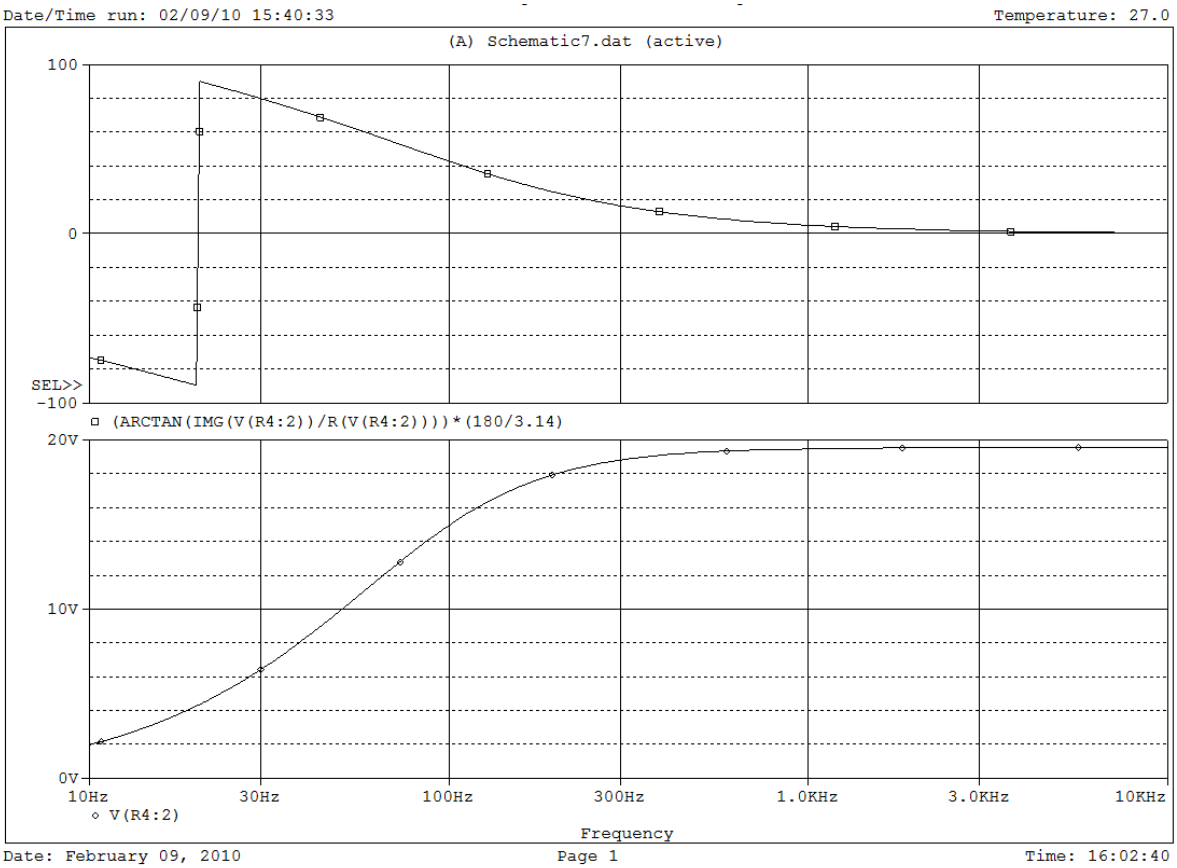
$$f = \frac{1}{2\pi RC}$$

$$100Hz = \frac{1}{2\pi R_{E1} C_E} \Rightarrow C_E = 13\mu F$$

$$10Hz = \frac{1}{2\pi R_L C_O} \Rightarrow C_o = 4\mu F$$

$$10Hz = \frac{1}{2\pi Z_{in} C_I} \Rightarrow C_I = 2.7\mu F$$

RESULTS: From what we can see above, C_O and C_I were smaller than C_E, and all of them were reasonable values. This was enough to work with until the values are simulated. Upon simulation, the values were adjusted to reflect standard values available for the practical circuit. On the next page are the bode plot, and the plot of the phase angle. Both demonstrate the requirements of the design. Notice, specifically, the value of the corner frequency; it is just about 100Hz, which was the target corner



frequency.

On top if the phase angle vs. frequency, and on the bottom is the voltage vs. frequency, which shows the corner frequency at about 100Hz.

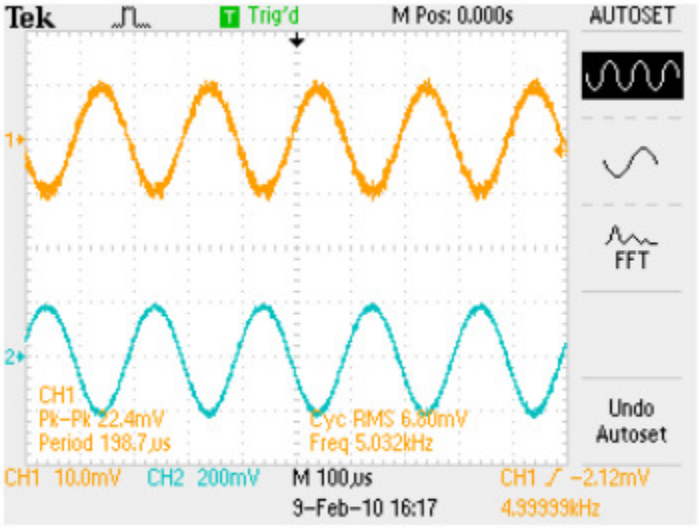
It is also important to note the operating point acquired for the .out file of the PSpice simulation. By inspection, one can see that the values calculated and the PSpice values were quite close.

TASK 7:

ANALYSIS: By building slowly and carefully, we were able to simulate the circuit on the Protoboard. The following values were used in place of the calculated values, since not all of them were available.

Name	Calculated Value	Practical Value
R_1	27.5kΩ	27kΩ
R_2	12.4kΩ	12kΩ
R_{E1}	120Ω	120Ω
R_{E2}	1.82kΩ	1.8kΩ
R_C	3.9kΩ	3.9kΩ
R_L	10kΩ	10kΩ
C_E	13µF	15 µF
C_O	4 µF	4.7 µF
C_I	2.7 µF	2.2 µF

RESULTS: Using the oscilloscope and function generator, we were able to verify the gain at, above and below 100Hz. The gain was -20 above 100Hz, slightly less at 100Hz, and about 10 at 50Hz. This verified the lower corner frequency was indeed at 100Hz. Below is a scope screen capture, as verification that the gain was about -20 above 100Hz.



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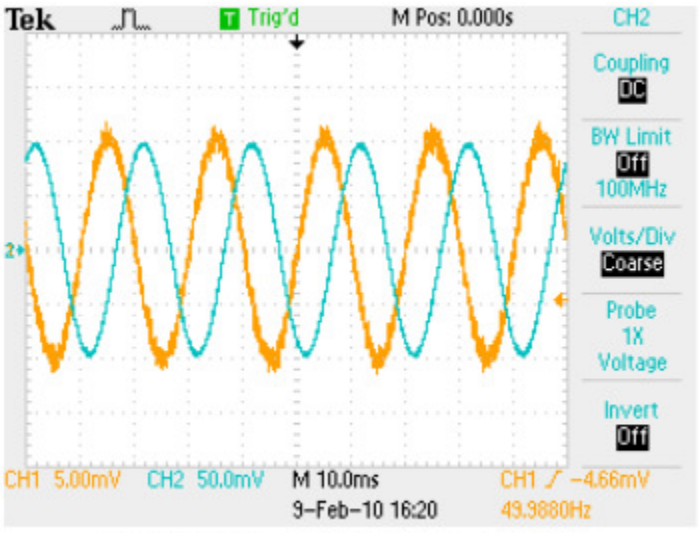
This image confirms that at frequencies above 100Hz, the gain is -20. Also, this screen capture was taken at a mid-band frequency between 1kHz and 10kHz, namely 5kHz. The gain here is measured at -20, and the input resistance measured 6.48kΩ.



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This screen capture demonstrates the gain degeneration at frequencies below 100Hz. At the frequency of 50Hz, there this was captured, the gain is about -10. The phase angle isn't correct, and the gain is half of what it should be.

TASK 8:

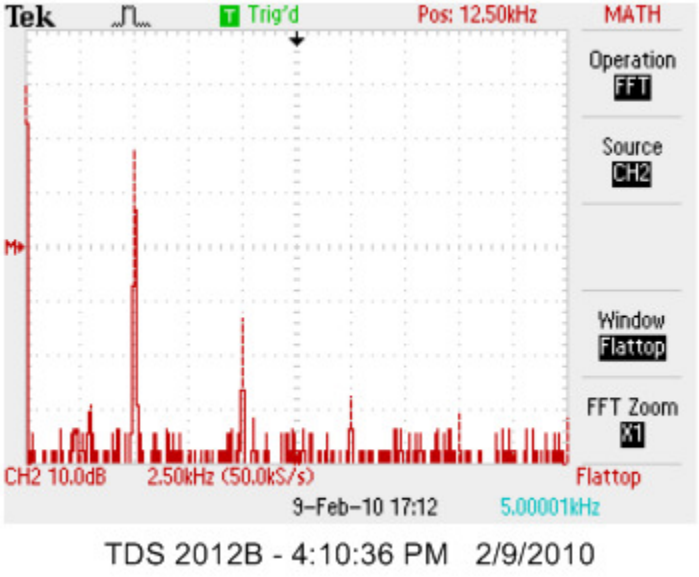
ANALYSIS: Normally, our system would be linear and time-invariant; however, since a non-linear device is in use, there is some small distortion. Total harmonic distortion is the measure of that distortion in the system. In order to calculate the harmonic distortion of the system, the FFT view of the oscilloscope must be used. More details can be found in the results section.

DATA AND CALCULATION: There is a great deal of calculation which goes into the harmonic distortion, and it involves the FFT graph in the results section. The method for calculation is as follows: Take the square root of the sum of the squares of harmonic component voltages. This is because power is proportional to the square of the voltage, and normally the distortion would be calculated with power.

$$THD = \%2.833, \pm 1V$$

$$THD = \%1.467, \pm 2V$$

RESULTS: The following shows the FFT plot for the system, which is used in the calculation of THD.



As you can see from the calculations above and the FFT, the distortion of the output is minimal. There are very clear harmonics, but they do not cause high distortion.

TASK 9:

ANALYSIS: The non-linearity of the system can be expressed as a Taylor Series.

RESULTS: With knowledge of the Taylor Series overall, it is simple to express the AC current i_C as a Taylor polynomial. Firstly, the system must be expressed as a Taylor polynomial, then it must be related to i_C.

$$e^{\frac{V_{be}}{V_T}} = \sum_{n=0}^{\infty} \frac{1}{n!}\left(\frac{V_{be}}{V_T}\right)^n, \qquad i_C = I_C e^{\frac{V_{be}}{V_T}}$$

$$\therefore \quad i_C = \frac{\sum_{n=0}^{\infty} \frac{1}{n!}\left(\frac{V_{be}}{V_T}\right)^n}{I_C}$$

$$OR \quad i_C = \frac{1 + \frac{V_{be}}{V_T} + \frac{1}{2}\left(\frac{V_{be}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_{be}}{V_T}\right)^3 + \frac{1}{24}\left(\frac{V_{be}}{V_T}\right)^4 + \cdots}{I_C}$$

Thus, the nonlinearity of the voltage gain could be expressed.

CONCLUSION:

In sum, this lab looked at many aspects of amplifier design, and guided us through the process, from choosing the bias current all the way to building the circuit. It is important to remember the specifications of the design when building the circuit, as reflected in the numerous expressions and definitions. Ultimately, however, having considered the restrictions, there is still a great number of possible configurations. There is no unique answer when designing the amplifier circuits. Interestingly, this circuit was, looking back, relatively easy to design. The restrictions were relatively non-conflicting, making it easy to choose values. Also, the chosen values were close to standard values, so even the simulations were accurate. Moreover, designs with more transistors may multiply in complexity, so it is important to take away the basics for design from this lab before moving on.