ELE339, Electronics I Laboratory

LAB 6

Bipolar Junction Transistor (BJT) Biasing

Objective:
The purpose of a biasing circuit is to establish an operating for the BJT, which provides linear operation and good stability with regard to variations of temperature as well as manufacturing parameters (e.g. β). We will investigate three resistive biasing schemes in this lab. An alternative biasing scheme predominantly used in integrated circuits is utilizing a *current mirror*. In this case, the desired operating current is imposed by creating a reference branch current, which is established by a well matched identical BJT device. Since the device in the reference branch features the same base emitter voltage, its current will closely match the operating current of the actual gain stage → current mirror.

Resistive Biasing:
Figure 1 shows the 3 most common resistive biasing schemes for BJTs.

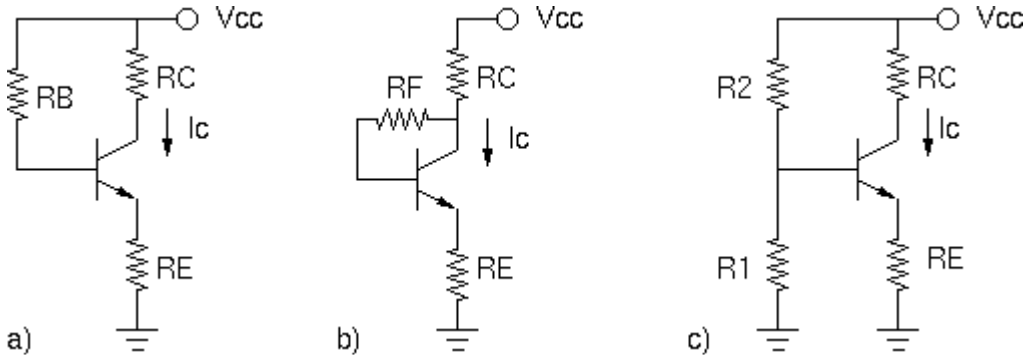

Figure 1: Three resistive biasing circuits for an NPN Transistor.

Note that the three depicted circuits only show the dc or Quiescent-point (Q-point) circuitry. In a practical application, all 3 schematics need to be complemented by some ac circuitry such as an ac input source and some decoupling capacitors at the input and output, respectively. However, since we assume *linear* operation, *superposition* applies and we can ignore all ac elements in our dc considerations.
Before we analyzed the depicted circuits, it is important to recall that the actual operating currents and the desired *collector-emitter* voltage are the designer's choice. Practically, the application may limit our choices, but there still remains some flexibility as to the exact dc parameter values. In this lab, we aim at a collector current of **1mA** and a collector-emitter voltage of approximately 5V (**Vcc=10V**). Furthermore, since the BJT is expected to be operated in the forward active mode, we possess a good estimate of its *base-emitter* voltage (0.6-0.7V for Silicon devices). Finally, we assume that all three emitter resistors are equal to 1kΩ.

Tasks:

1. Find the values for RB and RC in circuit a) that best meet the desired operating point values ($I_C \approx 1mA$, $V_{CE} \approx 5V$). To do so, assume that the BJT features a nominal current gain of $\beta=200$.
2. Find the minimum and the maximum collector current if β varies between 100 and 400. Is this solution acceptable (in terms of the maximum Q-point variation)?
3. Verify your theoretical results with PSpice.
4. Find RF and RC for circuit b), repeat your calculations in part 2 and verify your results with PSpice. Is this circuit better?
5. Find R1, R2 and RC for circuit c), repeat part 2 and verify your results with PSpice. Is this solution better than the previous two circuits?
6. If our circuits are exposed to large temperature variations, we can no longer ignore the resulting change in the base-emitter voltage. The latter drops by approximately 2mV for each 1C increase in (junction) temperature. How much would the collector current of each circuit change if the temperature were to increase by 50C (e.g. from 25C to 75C)?
7. Verify your results in 6 with the help of PSpice. Which circuit would you prefer with regard to temperature stability?
8. Build the circuit of your choice and measure I_C and V_{CE} at room temperature. When building the circuit, round all element values to the nearest available ones. The available logarithmically scaled resistor values are: 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8 and 8.2. The maximum error based on element value rounding should thus be limited to 10%.