

ELE405: Digital Computer Design

Fall 2009 Syllabus

Instructor: Professor Jien-Chung Lo
 Kelley Annex A-221, X-42996, jcl@ele.uri.edu

Course Webpage: <http://www.ele.uri.edu/Courses/ele405>

Lecture: MWF 12:00-12:50, Kelley 102

Office Hours: MW 1

Textbooks:

1. "The Designer's Guide to VHDL," Peter J. Ashenden, 2nd Edition, Morgan Kaufmann Publishers, 2002. ISBN: 1-55860-674-2.
2. "Pygmy CPU Manual" available from class website

Reference Texts:

3. "Computer Systems Design and Architecture," V. P. Heuring and H. F. Jordan, 2nd Edition, Prentice Hall, 2004. ISBN: 0-13-048440-7.
1. "Rapid Prototyping of Digital Systems," J. O. Hamblen and M. D. Furman, 2nd Edition, Kluwer Academic Pub., 2001. ISBN: 0-7923-7439-8.
2. "Digital Design and Implementation with Field Programmable Devices," Z. Navabi, Kluwer Academic Pub., 2005. ISBN: 1-4020-8011-5.

Schedule

wk	dates	Lecture	Project
1	9/9,11	Computer Arch. review	Phase 1: ISA
2	9/14,16,18	Inst. Set Architecture	
3	9/21,23,25	Register transfer level	
4	9/28,30, 10/2	Computer arithmetic	Phase 2: datapath
5	10/5,7,9	Processor design	
6	10/12,14,16	Memory system design	
7	10/19,21, 23	Input and output	Phase 3: control unit
8	10/26,28,30	Peripheral devices	
9	11/2,4,6	Processor design (adv.)	
10	11/9,11,13	Input and output	Phase 4: CPU
11	11/16,18, 20	Verifications/testing	Phase 5: Final project
12	11/23,25	Communications, net...	
13	11/30, 12/2,4	Modern processors	
14	12/7, 9, 11	Embedded Eng.	
15	12/18	Final Examination 8-11AM	

Grading Policy:

Project reports (phase 1-4)	50%	(phase1=10%, phase2=15%, phase3=15%, phase4=10%)
Quizzes	20%	
Final oral presentation/slides	10%	
Final project written report	20%	(phase5 included here)

Project track:

Phases 1 to 4 of the semester project are about the design and implementation of students' own CPUs. These should be conducted in teams of no more than two students. Usually, the team members in the laboratory track also work together for the project. At the end of each phase of the project, each team will submit a written report.

The last phase of the project will have five weeks of time. Each team will build a prototype of "real-life" computer-based systems, using their own CPU. There is no more scheduled lab during the last three weeks. However, students are required to attend the lab working on the project.

A list of potential project topics and ideas will be circulated early in the semester. Students are welcome to propose their own potential topics and ideas. This final phase of project will produce a working prototype similar to a real-life product. Demonstration and presentation will be conducted at the end of semester.

Course Outcomes:

1. Ability to analyze the performance of computer systems (a).
2. Ability to design, implement and debug complex digital systems with synthesis tools. As well as analyze their performance and devise an improvement (b).
3. Ability to design specifications for a computer and then design a computer that meets the specifications (c).
4. Ability to evaluate the trade-offs in computer design selections and to make decision based on various considerations using modern EDA tools (e, k,l).
5. Ability to lead and to be lead in a team working toward a common goal (d).
6. Recognize the need, and have the ability to carry out life-long learning (i).
7. Prepare written lab reports; written and oral presentation of final project (g).

For students with special needs:

Any student with a documented disability is welcome to contact me early in the semester so that we may work out reasonable accommodations to support your success in this course. The grading policy will remain the same as stated above. One should also contact Disability Services for Students, Office of Student Life, 330 Memorial Union, 874-2098.

ELE406: Digital Computer Design Laboratory

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Instructor: Professor Jien-Chung Lo
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Course Webpage: <http://www.ele.uri.edu/Courses/ele405/labs>
Course FTP: <ftp://ftp.ele.uri.edu/outgoing/jcl/405/>
Labs: M 2:00-4:45, Kelley 220

Class Materials: Lab manuals are available from course website. Archived design examples are available from the FTP site.

Schedule

wk	dates	Labs	Lab titles
1	9/14	Lab1	Pygmy CPU Simple Demo
2	9/21		
3	9/28		
4	10/5	Lab2	Video display and keyboard support
5	10/12		
6	10/19	Lab3	DE2 SRAM
7	10/26		
8	11/2	Lab4	Pygmy CPU with interrupts
9	11/9		
10	11/16		
11	11/23	Project	Build your own computer system
12	11/30		
13	12/7		
15	12/18	Final Examination 8-11AM	

Documentation of **PYGMY CPU** is available at
<http://www.ele.uri.edu/courses/ele405/f08/Pygmy.pdf>

Grading Policy:

Laboratory reports (x4) 75% (lab1=20%, lab2=15%, lab3=15%, lab4=25%)
Project Final reports 25%