QAM AND 4-PSK

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ACHIEVEMENTS: *review of the quadrature amplitude modulator (QAM) in digital communications; as a generator of a quadrature phase shift keyed (QPSK, or 4-PSK) signal. Demodulation of QPSK.*

PREREQUISITES: *it would be advantageous to have completed some of the experiments of Volume A1 involving linear modulation and demodulation, as well as the experiment entitled* ***Phase division multiplex*** *in Volume A2.*

ADVANCED MODULES: *DECISION MAKER. A total of three MULTIPLIER modules is required.*

TRUNKS: *see your Laboratory Manager about the QPSK signal(s) at TRUNKS*

PREPARATION

the QAM principle

Recall the experiment entitled *Phase division multiplex* in Volume A2. Two double sideband suppressed carrier (DSBSC) signals were combined on a common carrier (and so a common channel), by adding (multiplexing) them in phase-quadrature. In the analog environment the two analog messages are independent, and the signal is called quadrature amplitude modulation - QAM.

The QAM modulator was of the type shown in Figure 1 below. The two paths to the adder are typically referred to as the 'I' (inphase), and 'Q' (quadrature), arms.

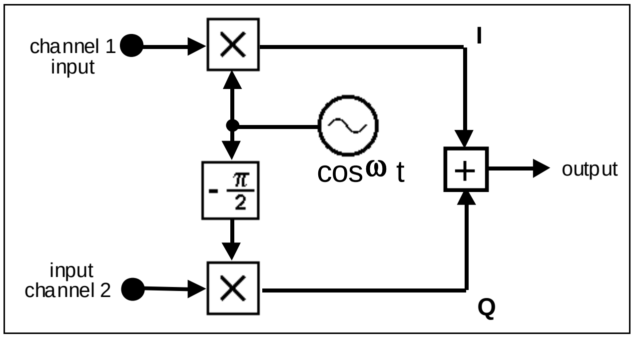

Figure 1: a quadrature modulator

Not shown in Figure 1 is any bandlimiting. In a practical situation this would be implemented either at message level - at the input to each multiplier - and/or at the output of the adder. Probably both !

The motivation for QAM comes from the fact that a DSBSC signal occupies twice the bandwidth of the message from which it is derived. This is considered wasteful of resources. QAM restores the balance by placing two independent DSBSC, derived from message #1 and message #2, in the same spectrum space as one DSBSC. The bandwidth imbalance is removed.

In digital communications this arrangement is popular. It is used because of its bandwidth conserving (and other) properties.

It is not used for multiplexing two independent messages. Given an input binary sequence (message) at the rate of n bit/s, two sequences may be obtained by splitting the bit stream into two paths, each of n/2 bit/s. This is akin to a serial-to-parallel conversion.

The two streams become the channel 1 and channel 2 messages of Figure 1.

Because of the halved rate the bits in the I and Q paths are stretched to twice the input sequence bit clock period.

The two messages are recombined at the receiver, which uses a QAM-type demodulator.

The two bit streams would typically be band limited and/or pulse shaped before reaching the modulator.

A block diagram of such a system is shown in Figure 2 below.

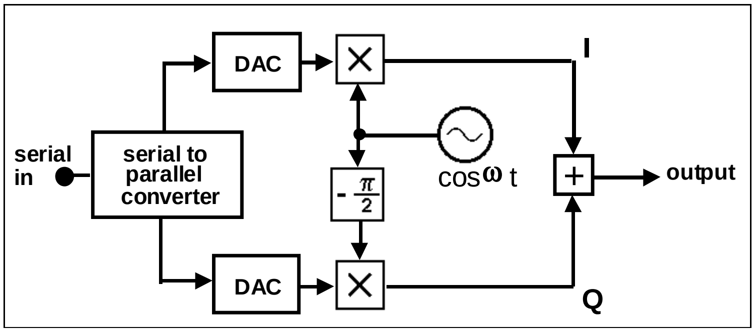

Figure 2: a QPSK modulator

QAM becomes QPSK

The QAM modulator is so named because, in analog applications, the messages do in fact vary the amplitude of each of the DSBSC signals.

In QPSK the same modulator is used, but with binary messages in both the I and Q channels, as describe above.

Each message has only two levels, ±V volt. For a non-bandlimited message this does not vary the amplitude of the output DSBSC. As the message changes polarity this is interpreted as a 180^0 phase shift, given to the DSBSC.

Thus the signal in each arm is said to be undergoing a 180^0 phase shift, or phase shift keying - or PSK.

Because there are two PSK signals combined, in quadrature, the two-channel modulator gives rise to a quadrature phase shift keyed - QPSK - signal.

constellation

Viewed as a phasor diagram (and for a non-bandlimited message to each channel), the signal is seen to occupy any one of four point locations on the complex plane. These are at the corner of a square (a square lattice), at angles $\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$ to the real axis.

You will see this *signal constellation* later in the experiment.

M-PSK and M-QAM

The above has described digital-QAM or QPSK. This signal is also called 4-PSK or 4-QAM. More generally signals can be generated which are described as M-QAM or M-PSK.

Here $M = 2^{\mathbf{L}}$, where **L** = the number of levels in each of the I and Q arms. For the present experiment **L** = 2, and so M = 4.

The 'M' defines the number of points in the signal constellation.

For the cases $M > 4$ then M-PSK is not the same as M-QAM.

It is beyond the intended scope of this experiment to discuss these differences. But it is certainly worth your while to read further on the subject, and to discover the different constellations that these signals generate.

Refer to your text book for more detail.

See also the experiment entitled *Multi-level QAM and PSK* in this Volume.

the QAM receiver

The QAM receiver follows the similar principles to those at the transmitter, and is illustrated in idealised from in the block diagram of Figure 3.

It is idealised because it assumes the incoming signal has its two DSBSC precisely in phase quadrature. Thus only one phase adjustment is required.

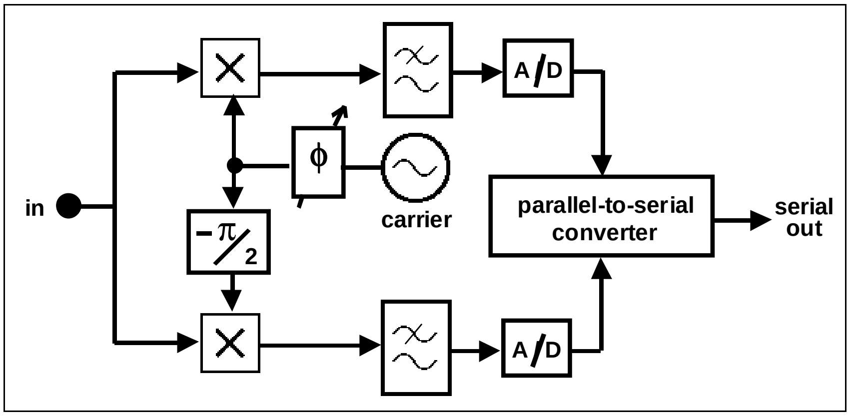

Figure 3: the QAM demodulator for QPSK

The parallel-to-serial converter block performs the following operations:

1. regenerates the bit clock from the incoming data. See, for example, the experiment entitled *Bit clock regeneration* in this Volume.
2. regenerates a digital waveform from both the analog outputs of the I and Q arms.
3. re-combines the I and Q signals, and outputs a serial data stream.

Not shown is the method of carrier acquisition. This ensures that the oscillator, which supplies the local carrier signal, is synchronized to the received (input) signal in both frequency *and* phase.

experiment simplification

You are familiar with the practice of using a stolen carrier. This enables you to concentrate on a particular aspect of a system, without being obliged to spend time becoming involved with carrier acquisition, which can be a complex process.

For an experiment explicitly concerned with the acquisition of a carrier from such a signal, see the experiment entitled *The Costas loop* (Volume A2), and *Carrier acquisition* (in Volume D2).

Likewise, in this experiment, it is not necessary to become involved with details which are not of direct relevance. So two independent data sequences will be used at the input to the modulator, rather than having digital circuitry to split one data stream into two (the serial-to-parallel converter).

For the purposes of demonstration the above mentioned techniques simplify the model.

Two such independent data sequences, sharing a common bit clock (2.083 kHz), are available from a single SEQUENCE GENERATOR module. The data stream from which these two channels are considered to have been derived would have been at a rate of twice this - 4.167 kHz.

Lowpass filter bandlimiting and pulse shaping is not a subject of enquiry in this experiment. So a single bandpass filter at the ADDER (summer) output will suffice, providing it is of adequate bandwidth. A 100 kHz CHANNEL FILTERS module is acceptable (filter #3).

EXPERIMENT

the QPSK transmitter

A model of the generator of Figure 1 is shown in Figure 4.

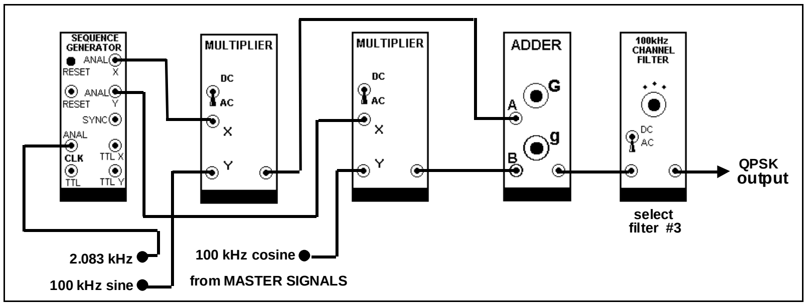

Figure 4: the QAM modulator for QPSK

The QAM modulator involves analog circuitry. Overload must be avoided, to prevent crosstalk between channels when they share a common path - the ADDER and output filter. In practice there would probably be a filter in the message path to each multiplier. Although these filters would be included for pulse shaping and/or band limiting, a secondary purpose is to eliminate as many unwanted components at the multiplier (modulator) input as possible. See Tutorial Question Q7.

T1 *patch up the modulator according to Figure 4. Set the on-board switch SW1 of the PHASE SHIFTER to HI. Select channel #3 of the 100 kHz CHANNEL FILTERS module (this is a bandpass filter of adequate bandwidth).*

T2 *there are no critical adjustments to be made. Set the signals from each input of the ADDER to be, say, 1 volt peak at the ADDER output. See Tutorial Question Q5.*

T3 *for interest predict the waveforms (amplitude and shape) at all interfaces, then confirm by inspection. What will be a suitable oscilloscope trigger in each case ?*

constellation

You can display the four-point constellation for QPSK:

T4 *set the oscilloscope in X-Y mode. With no input, select equal gains per channel. Locate the 'spot' in the centre of the screen; then connect the two data streams entering the QAM to the scope X and Y inputs.*

How would the display change if each of the data streams, presently non-bandlimited, was first passed through a bandlimiting filter ? Try this with the LPF in the HEADPHONE AMPLIFIER and a TUNEABLE LPF.

the demodulator

Modelling of the demodulator of Figure 3 is straightforward. But it consumes a lot of modules. Consequently only one of the two arms is shown in Figure 5.

If you have insufficient modules to retain your QPSK modulator, then you can use a QPSK signal supplied at TRUNKS with which to test your demodulator.

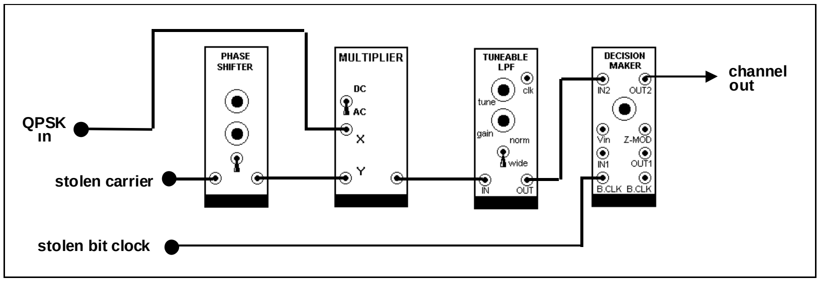

Figure 5: one channel of the demodulator

The PHASE SHIFTER can be used to select either channel from the QAM signal. If both channels re required simultaneously, as in practice, then a second, identical demodulator must be provided.

T5 *patch up the single channel demodulator of Figure 5, including the z-mod facility of the DECISION MAKER. Use an eye pattern to locate the optimum decision point.*

T6 *while watching the 'I' channel at the transmitter, use the PHASE SHIFTER to match the demodulator output with it.*

T7 *while watching the 'Q' channel at the transmitter, use the PHASE SHIFTER to match the demodulator output with it.*

TUTORIAL QUESTIONS

Q1 *explain how a QAM system conserves bandwidth.*

Q2 *how would you measure the phase between two DSBSC ? Would a basic* PHASE METER*, which is used for indicating the phase between two sinewaves, be of any help ?*

Q3 *the modulator used the quadrature 100 kHz outputs from the MASTER SIGNALS module. Did it matter if these were not* ***precisely*** *in quadrature ? Explain.*

Q4 *the demodulator did not rely on the phasing of the 100 kHz quadrature outputs from the MASTER SIGNALS module, but instead required some means of phase adjustment of the carriers into* ***both*** *MULTIPLIER modules. Explain.*

Q5 *in the modulator, if each signal at the ADDER output is 1 volt peak, what will be the peak amplitude of their sum ?*

Q6 *name one advantage of making the bit rate a sub-multiple of the carrier frequency.*

Q7 *why is there a need to eliminate as many unwanted components as possible into the modulator ?*