A Novel High-Performance CMOS 1-Bit Full-Adder Cell

Ahmed M. Shams and Magdy A. Bayoumi

Abstract—A novel 16-transistor CMOS 1-bit full-adder cell is proposed. It uses the low-power designs of the XOR and XNOR gates [1], pass transistors, and transmission gates. The cell offers higher speed and lower power consumption than standard implementations of the 1-bit full-adder cell. Eliminating an inverter from the critical path accounts for its high speed, while reducing the number and magnitude of the cell capacitances, in addition to eliminating the short circuit power component, account for its low power consumption. Simulation results comparing the proposed cell to the standard implementations show its superiority. Different circuit structures and input patterns are used for simulation. Energy savings up to 30% are achieved.

Index Terms—Binary addition, full adder, high speed, low power.

I. INTRODUCTION

Most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. Addition, subtraction, multiplication, and multiply and accumulate (MAC) are examples of the most commonly used operations. The 1-bit full-adder cell is the building block of all these modules. Thus, enhancing its performance is critical for enhancing the overall module performance. The most important performance parameters for future VLSI systems are speed and power consumption. In this paper we present a novel 1-bit full-adder cell which offers faster operation, and consumes less power than standard implementations of the full-adder cell.

The rest of this paper is organized as follows, in Section II we discuss power consumption issues in CMOS VLSI circuits. In Section III, we review some standard implementations of the full-adder cell. Then in Section IV, we present the novel 1-bit full-adder cell and analyze its performance. Finally, in Section V, we present simulation results, which show the superiority of the proposed cell.

II. POWER CONSUMPTION IN CMOS VLSI CIRCUITS

There are three main components of power consumption in digital CMOS VLSI circuits.

1) Switching Power: consumed in charging and discharging of the circuit capacitances during transistor switching.
2) Short-Circuit Power: consumed due to short-circuit current flowing from power supply to ground during transistor switching.
3) Static Power: consumed due to static and leakage currents flowing while the circuit is in a stable state.

The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits [2], [3]. It depends on the input pattern applied to the circuit, which will either cause the transistors to switch (circuit capacitances consume power) or to keep their previous state (no power consumption) at each clock cycle. The third component is usually negligible in a well-designed CMOS circuit [3].

The total power is given by the following equation [4]:

\[ P_{\text{total}} = V_{dd} \cdot f_{\text{clk}} \cdot \sum_i V_{\text{swing}_i} \cdot C_{i,\text{load}} \cdot p_i + V_{dd} \cdot \sum_i I_{i,\text{cc}} + V_{dd} \cdot I_{i,\text{leak}} \]

where

- \( V_{dd} \) power supply voltage;
- \( V_{\text{swing}_i} \) voltage swing of the output which is ideally equal to \( V_{dd} \);
- \( C_{i,\text{load}} \) load capacitance at node \( i \);
- \( f_{\text{clk}} \) system clock frequency;
- \( I_{i,\text{cc}} \) switching activity at node \( i \);
- \( I_{i,\text{leak}} \) leakage current.

The summation is over all the node capacitances of the circuit.

With the constant increase in systems’ clock frequency, designing systems with low power consumption is not a straightforward task, as it involves different system abstraction levels. Beginning from system behavioral description and ending with fabrication process and packaging, all the steps can be tailored toward low power design. In this paper, low power consumption is targeted at the circuit level. Reducing the number and magnitude of the circuit capacitances, reducing the voltage swing at some internal nodes, and reducing the spurious transitions in the output signal are some of the techniques used at the circuit level to reduce the power consumption.

III. STANDARD IMPLEMENTATIONS OF THE 1-BIT FULL ADDER CELLS

The 1-bit full-adder functionality can be summarized by the following equations, given the three 1-bit inputs \( A \), \( B \), and \( C_{in} \), it is desired to generate the two 1-bit outputs Sum and \( C_{out} \), where

\[ \text{Sum} = (A \text{ XOR } B) \text{ XOR } C_{in} \]
\[ C_{out} = A \cdot B + C_{in} \cdot (A \text{ XOR } B). \]

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Standard implementations of the 1-bit full-adder cells that are the transmission gates full-adder cell (TGA), shown in Fig. 1(a), which is based on the CMOS transmission gates and has 20 transistors [5], and the transmission function full-adder cell (TFA), shown in Fig. 1(b), which is based on the transmission function theory and has 16 transistors [6].

Both of these cells generate the **XOR** function ($H = A \text{XOR} B$), followed by an inverter to generate the **XNOR** function ($H'$). Both $H$ and $H'$ are used to control the transmission gates generating the Sum and $C_{\text{out}}$ outputs. The inverter introduces unwanted delay between $H$ and $H'$ leading to a 0–0 or 1–1 overlap. This overlap will cause the transmission gates to act as pass transistors, which may cause glitches (spurious transitions) in the output signals. These glitches will increase the power consumption of these cells. In addition, TGA uses three inverters, while TFA uses two. The presence of inverters will introduce short-circuit power due to the current flowing from the power supply to ground (when both $P$ and $X$ transistors are instantaneously on).

TFA has been proved to outperform TGA in [7], [8]. One of the recent enhancements is the 14-transistors adder (14T) presented in [7]. Power consumption has been reduced by using the 4-transistor XOR implementation presented in [1], which decreases the overall cell transistor count to 14 (see Fig. 2). 14T uses only one inverter, but it still has the same problem of glitches in the outputs. Also, it has the drawback of introducing a static power component at the inverter output. Due to the incomplete voltage swing of the XOR gate when $A = B = 0$, both the $X$ and $P$ transistors will be on ($X$ is weakly on), which will lead to drawing current from the power supply although the circuit is in steady state. This drawback increases the power consumed by this cell, but still it remains a good candidate for low power applications due to having only 14 transistors. Other adder cells are discussed in [9] and [10], which have transistor counts ranging from 24 to 54 transistors. In this paper, we use TFA and 14T as a reference, and we compare their performance to our proposed cell.

**IV. THE PROPOSED 1-BIT FULL ADDER CELL**

The novel adder cell (NEW) has 16 transistors. It is based on the 4-transistor implementations of the **XOR** and **XNOR** functions presented in [1], pass transistor, and transmission gates. The cell is shown in Fig. 3. NEW simultaneously generates $H$ and $H'$. This new style has several advantages: first, it removes the inverter from the critical path of the cell, which decreases the cell delay. Second, it balances the delays of generating $H$ and $H'$, which leads to fewer glitches at the outputs. Third, it decreases the capacitance at node $H$, since it is no longer loading an inverter, while at the same time decreasing the capacitance at node $H'$. Also, it is noticed that NEW does not use any inverters or standard CMOS style. This eliminates the short-circuit power component within the cell (normally 5–20 of the dynamic power [11]). Finally, the incomplete voltage swing at $H$ and $H'$ for some input combinations ($A = B = 0, A = B = 1$) reduces the power consumed in the these transitions (The $V_{\text{swing}}$ term in this case is less than $V_{dd}$). Accordingly, the proposed cell NEW should consume less power than the standard adder cell implementations discussed earlier. The analytical reasonings are verified by circuit simulation in the following section.

**V. SIMULATION RESULTS**

The three 1-bit adder cells (TFA, 14T, and NEW) have been prototyped and simulated. Magic V6.5 with MOSIS SCN3ME_SUBM 0.35-μ technology file, and HSPICE have been used. The three inputs have been generated from buffers and have been fed into the adder cell, while the two outputs have been also loaded with buffers. This suitable input and output loading gives a more realistic simulation circuit structure. The cell delay has been measured from the moment the inputs reach 50% of the voltage supply level (after the input buffers) to the moment the latest of the Sum and $C_{\text{out}}$ signals reach the same voltage level (before the output buffers). All transitions from an input combination to another (56 patterns) have been tested, and the delay at each transition has been measured. The maximum has been reported as the cell delay. For power consumption measurements, a random-generated input pattern applied to the cells for a long time period has been used. The average power for the duration of this pattern has been reported as the cell power consumption figure.
Fig. 4. Snapshots of the input and output signals. Inputs A, B, C\textsubscript{in} are the top three rows, respectively. C\textsubscript{out} and S for cell 14T come next, followed by C\textsubscript{out} and S for TFA, and finally C\textsubscript{out} and S for NEW.

The simulation results are shown in Table I. The operating frequency is 1 GHz and the voltage supply is 3.3 V. NEW consumes 4.5\% less power than 14T and 9\% less than TFA. Regarding speed, NEW is superior; it is faster than 14T by 28\% and TFA by 8\%. The overall savings show that from the power-delay product (energy), it saves 26\% over 14T and 16\% over TFA. Snapshots of the input and output signals of the three cells are shown in Fig. 4, while plots of the power consumed by the three cells over time are shown in Fig. 5. The cells have also been tested in bigger circuit structures. A 4-bit ripple carry module, which is the building block of other larger adders, has been used. The simulation results for the three cells are shown in Table II. NEW has shown superior results as well. Energy savings of 24\% and 9\% are achieved over 14T and TFA, respectively. In a cascade of full-adder cells, the signals decay while passing through the series. Adding buffers whenever the signal is weak is a recommended idea, but this will increase the power consumption. It is not recommended to use any of the full adders discussed in this paper in cascades of more than four cells without adding intermediate buffers.

The 4-bit RCA building block for each cell has been used to build a 16-bit carry-select adder (CSA). The simulation results are shown in the second part of Table II. Energy savings of 30\% and 15\% are achieved over 14T and TFA, respectively. The results show that the speed and low power consumption of NEW are also verified in bigger circuits.

VI. CONCLUSION

A novel low-power 1-bit full-adder cell has been proposed. It uses the 4-transistor implementations of the XOR and XNOR functions, transmission gates, and pass transistors. Low power consumption is targeted at the circuit-design level. The cell is characterized by having no inverters and a balanced generation of the control signals of its transmission gates. It has a lower dynamic power component and no short-circuit
power component. Simulation results for the 1-bit cells, 4-bit ripple carry, and 16-bit carry select adders show the superiority of the proposed cell over standard implementations.

REFERENCES


