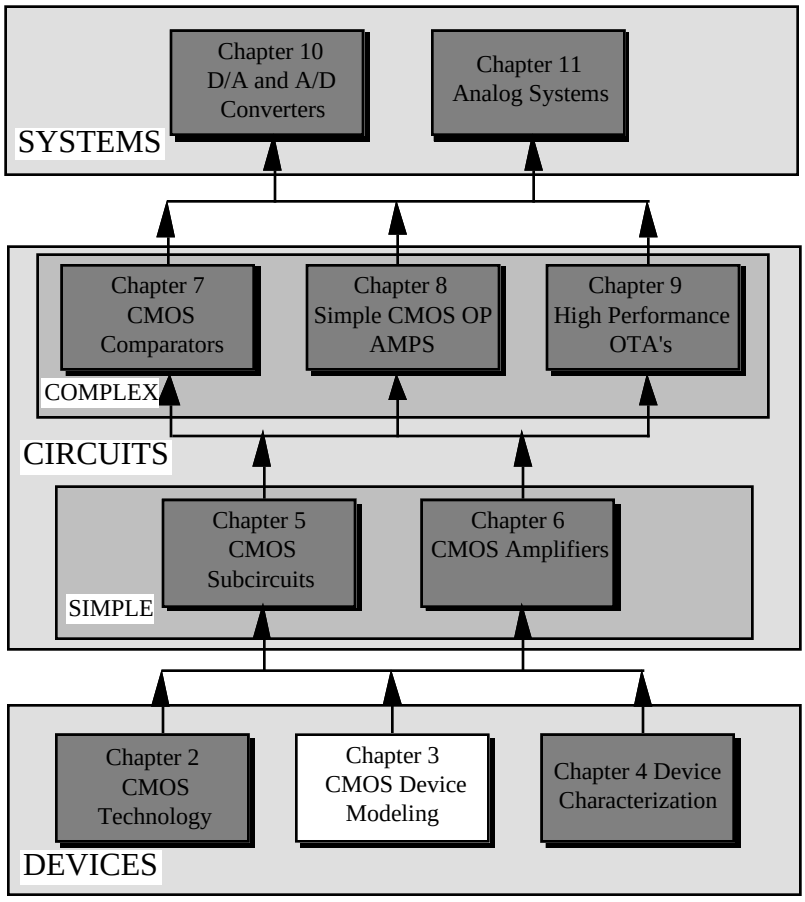
III. CMOS MODELS

Contents

Perspective



III.1 - MODELING OF CMOS ANALOG CIRCUITS

Objective

1. Hand calculations and design of analog CMOS circuits.
2. Efficiently and accurately simulate analog CMOS circuits.

Large Signal Model

The large signal model is nonlinear and is used to solve for the dc values of the device currents given the device voltages.

The large signal models for SPICE:

Basic drain current models -

1. Level 1 - Shichman-Hodges (V_T, K', γ, λ, ϕ, and N_{SUB})

2. Level 2 - Geometry-based analytical model. Takes into account second-order effects (varying channel charge, short-channel, weak inversion, varying surface mobility, etc.)

3. Level 3 - Semi-empirical short-channel model

4. Level 4 - BSIM model. Based on automatically generated parameters from a process characterization. Good weak-strong inversion transition.

Basic model auxilliary parameters include capacitance [Meyer and Ward-Dutton (charge-conservative)], bulk resistances, depletion regions, etc..

Small Signal Model

Based on the linearization of any of the above large signal models.

Simulator Software

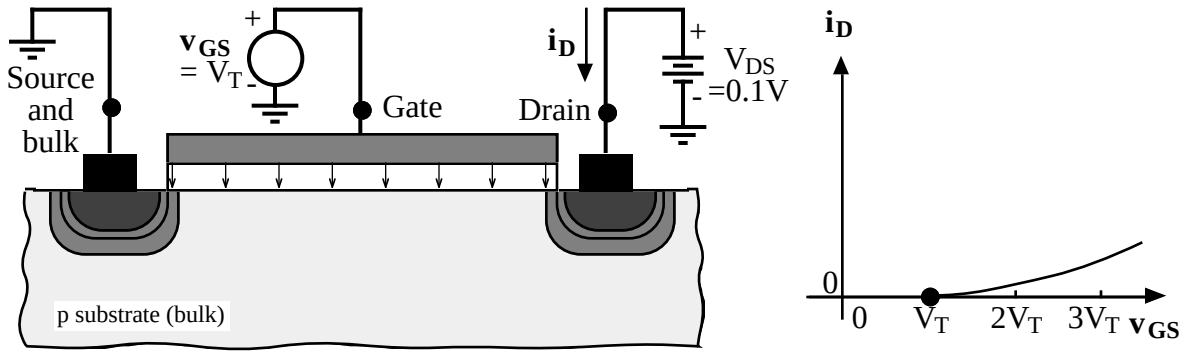
SPICE2 - Generic SPICE available from UC Berkeley (FORTRAN)

SPICE3 - Generic SPICE available from UC Berkeley (C)

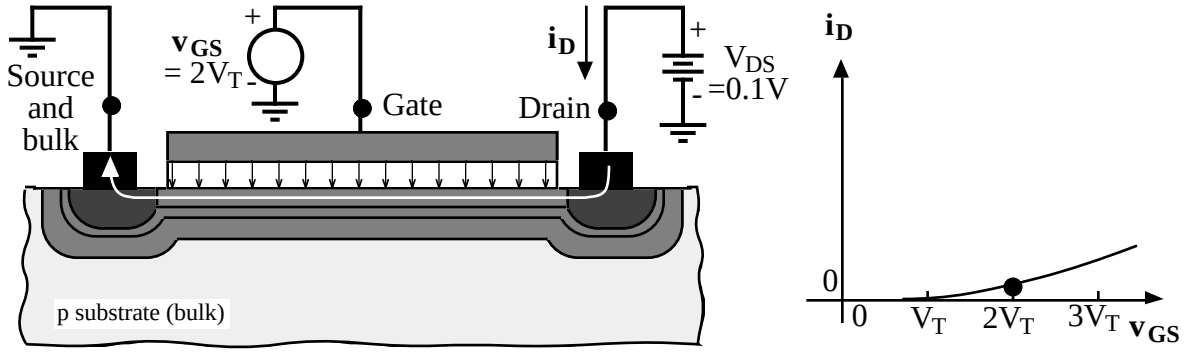
SPICE- Every other SPICE simulator!

Transconductance Characteristics of NMOS when V_{DS} = 0.1V

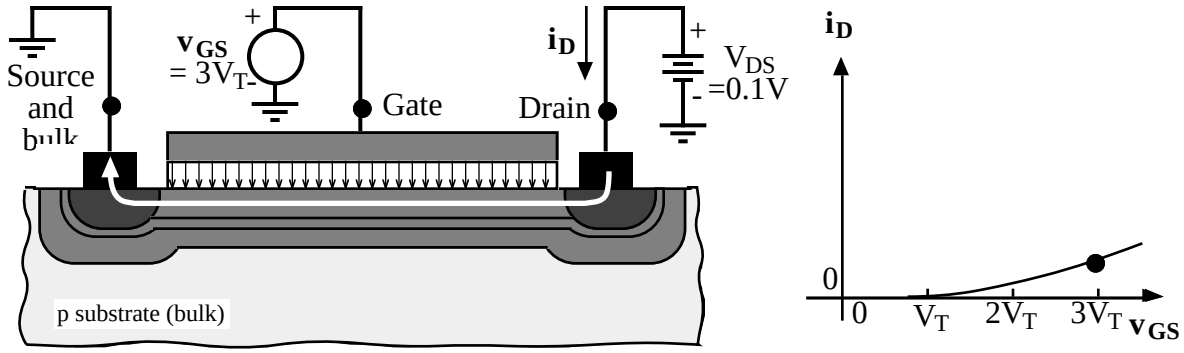
$v_{GS} \leq V_T$:



$v_{GS} = 2V_T$:

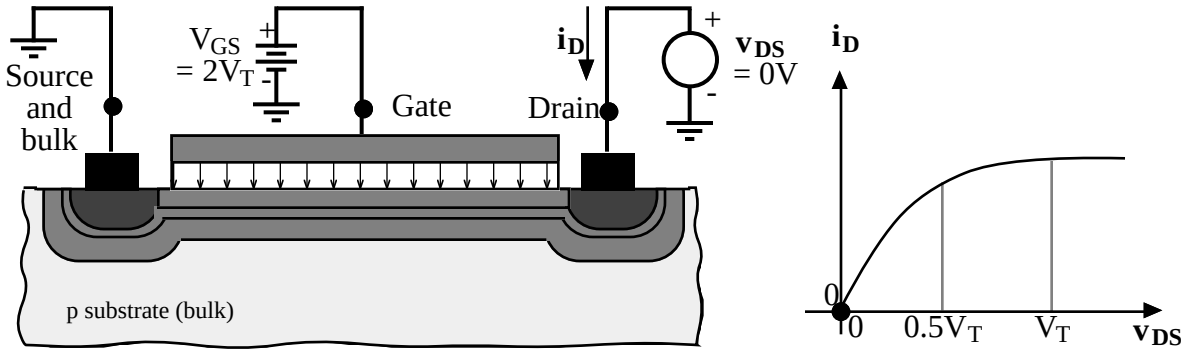


$v_{GS} = 3V_T$:

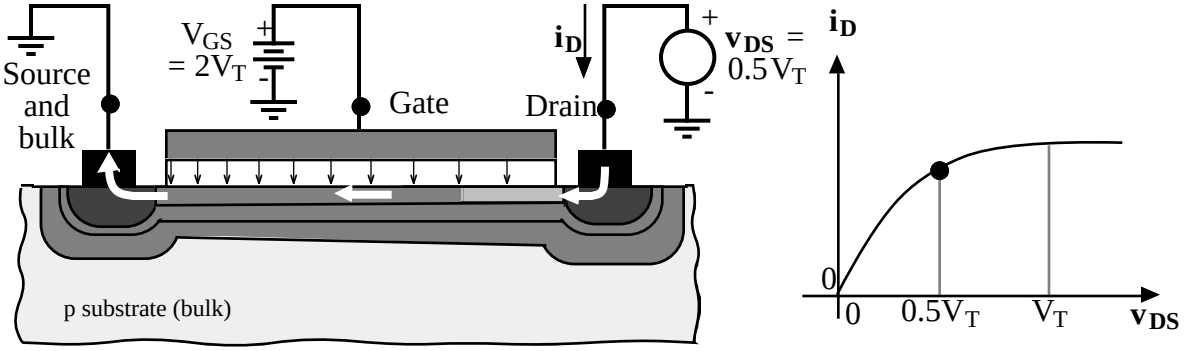


Output Characteristics of NMOS for $V_{GS} = 2V_T$

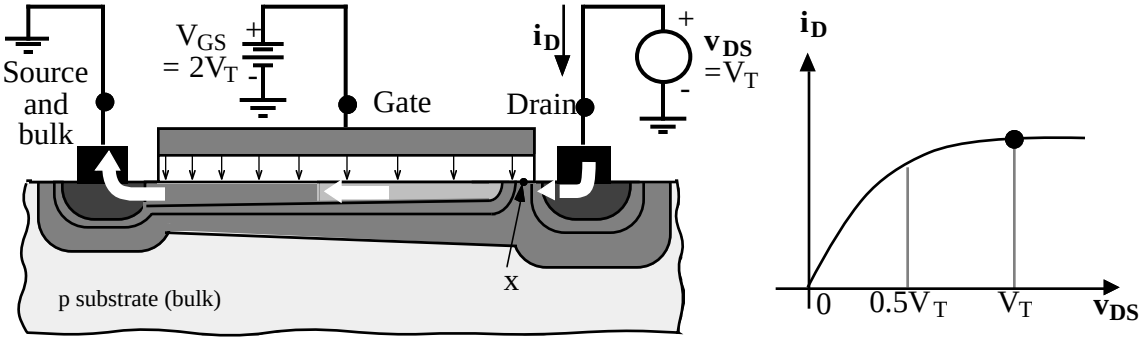
$v_{DS} = 0V$:



$v_{DS} = 0.5V_T$:

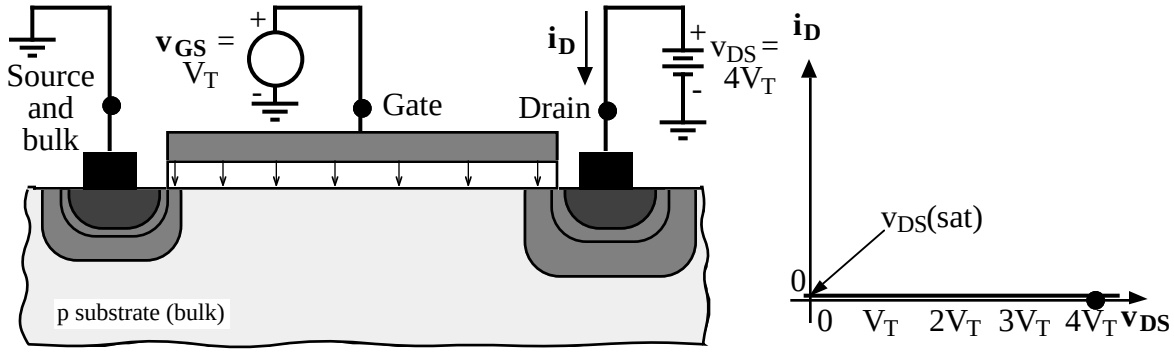


$v_{DS} = V_T$:

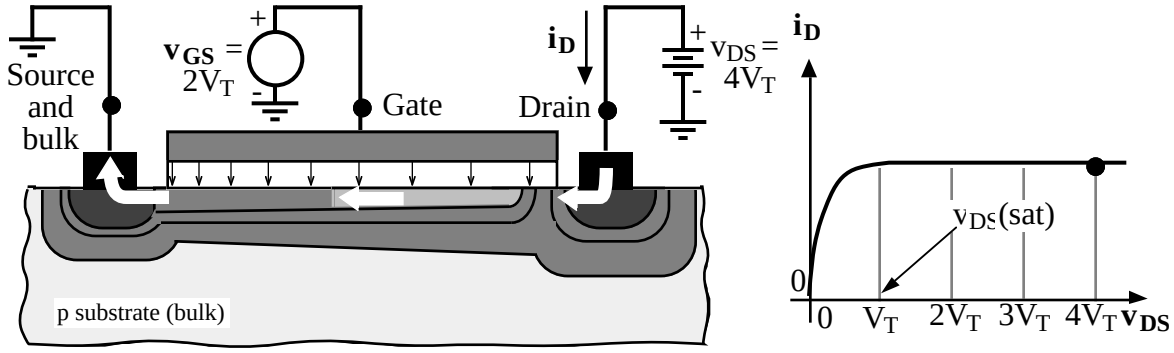


Output Characteristics of NMOS when $v_{DS} = 4V_T$

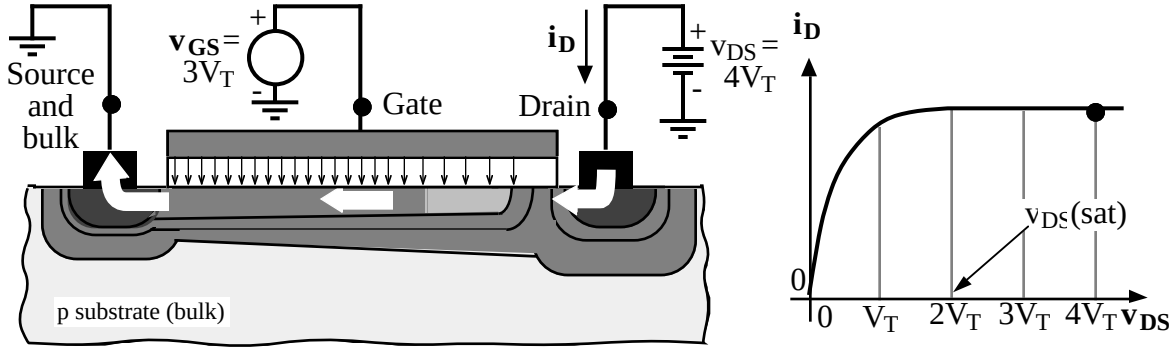
$v_{GS} = V_T$:



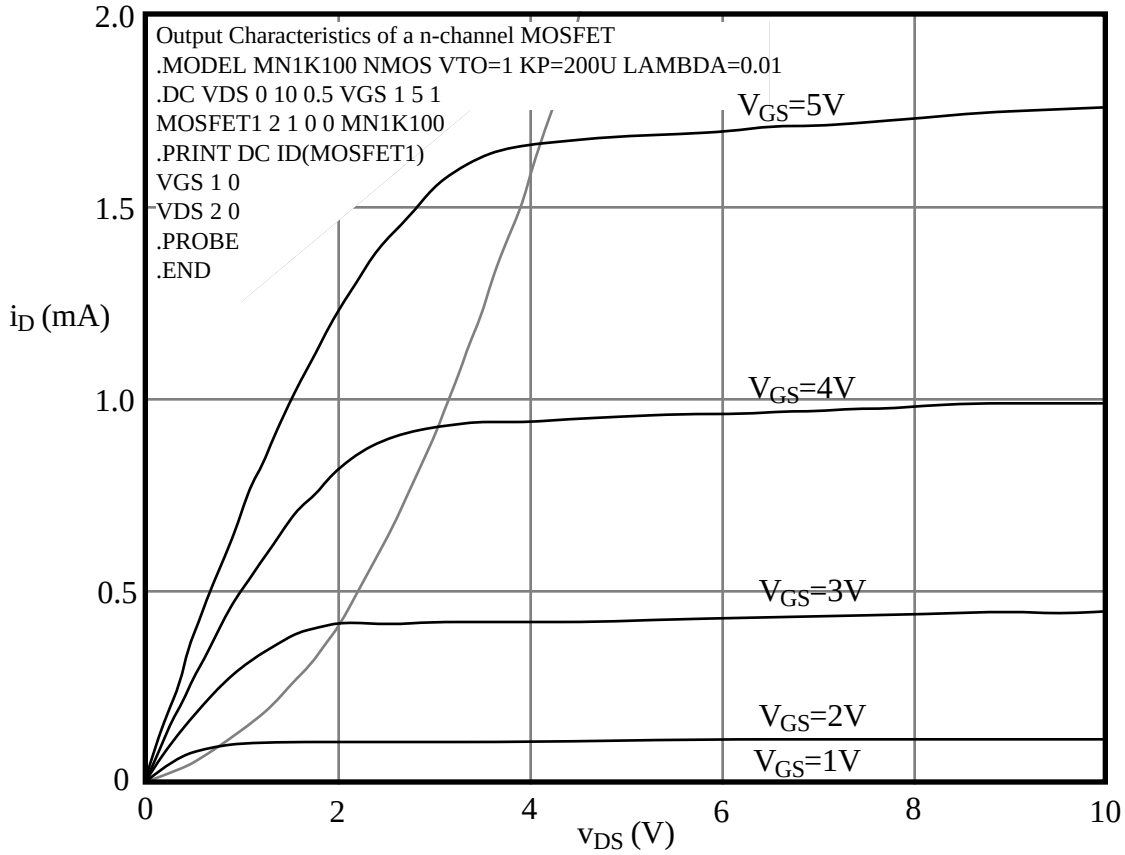
$v_{GS} = 2V_T$:



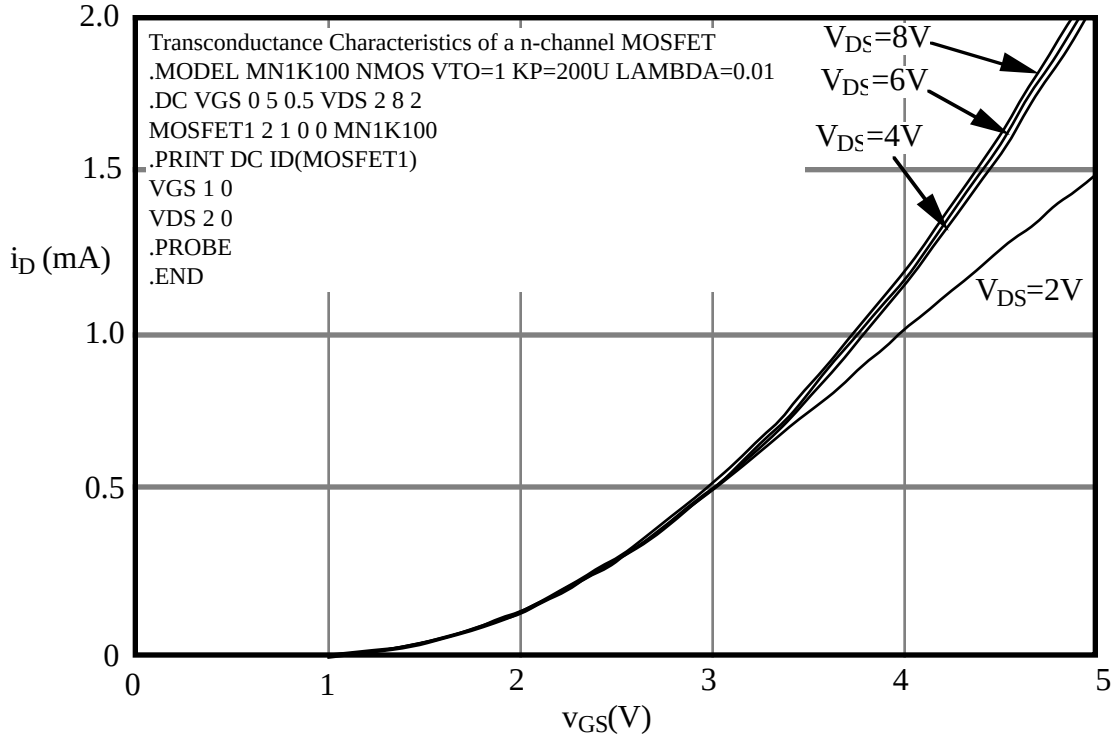
$v_{GS} = 3V_T$:



Output Characteristics of an n-channel MOSFET

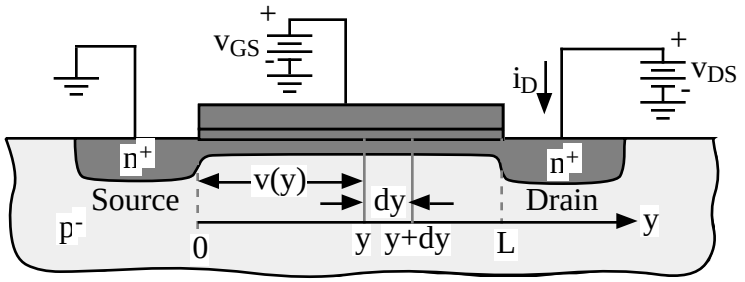


Transconductance Characteristics of an n-channel MOSFET



SIMPLIFIED SAH MODEL DERIVATION

Model-



Derivation-

- Let the charge per unit area in the channel inversion layer be

$$Q_I(y) = C_{ox}[v_{GS} - v(y) - V_T] \quad (\text{coulombs/cm}^2)$$

- Define sheet conductivity of the inversion layer per square as

$$\sigma_S = \mu_o Q_I(y) \quad \left(\frac{\text{cm}^2}{\text{v}\cdot\text{s}}\right)\left(\frac{\text{coulombs}}{\text{cm}^2}\right) = \frac{\text{amps}}{\text{volt}} = \frac{1}{\Omega/\text{sq.}}$$

- Ohm's Law for current in a sheet is

$$J_S = \frac{i_D}{W} = \sigma_S E_y = \sigma_S \frac{dv}{dy} \ .$$

Rewriting Ohm's Law gives,

$$dv = \frac{i_D}{\sigma_S W}\ dy = \frac{i_D dy}{\mu_o Q_I(y) W}$$

where dv is the voltage drop along the channel in the direction of y.

Rewriting as

$$i_D\ dy = W\mu_o Q_I(y) dv$$

and integrating along the channel for 0 to L gives

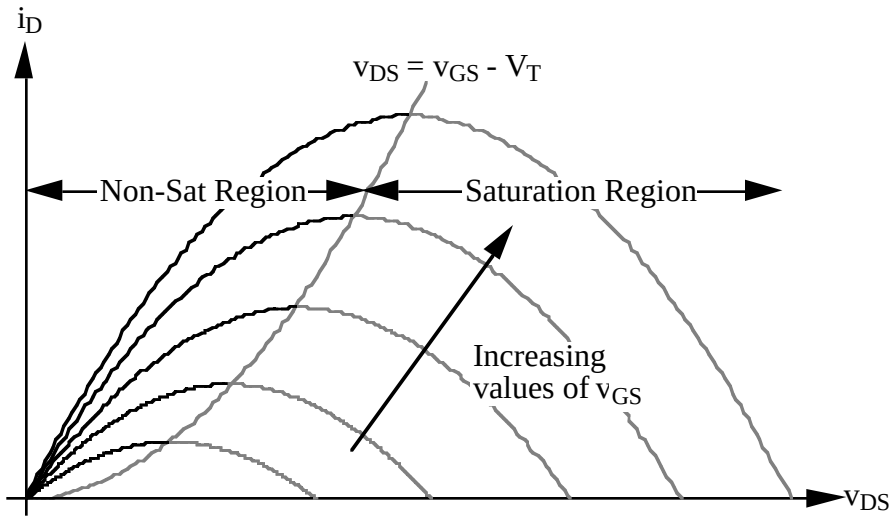
$$\int_0^L i_D dy = \int_0^{v_{DS}} W\mu_o Q_I(y) dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS} - v(y) - V_T]\ dv$$

After integrating and evaluating the limits

$$\boxed{i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

ILLUSTRATION OF THE SAH EQUATION

Plotting the Sah equation as i_D vs. v_{DS} results in -



Define $v_{DS}(sat) = v_{GS} - V_T$

Regions of Operation of the MOS Transistor

1.) Cutoff Region:

$i_D = 0, \quad v_{GS} - V_T < 0$

(Ignores subthreshold currents)

2.) Non-saturation Region

$$i_D = \frac{\mu C_{ox} W}{2L}\left[2(v_{GS} - V_T) - v_{DS}\right]v_{DS}\ ,\ 0 < v_{DS} < v_{GS} - V_T$$

3.) Saturation Region

$$i_D = \frac{\mu C_{ox} W}{2L}\left[(v_{GS} - V_T)^2\right],\ 0 < v_{GS} - V_T < v_{DS}$$

SAH MODEL ADJUSTMENT TO INCLUDE EFFECTS OF V_{DS} ON V_T

From the previous derivation:

$$\int_0^L i_D\,dy = \int_0^{v_{DS}} W\mu_o Q_I(y)dy = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS} - v(y) - V_T]dv$$

Assume that the threshld voltage varies across the channel in the following way:

$$V_T(y) = V_T + \Delta v(y)$$

where V_T is the value of the threshold voltage at the source end of the channel.

Integrating the above gives,

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v(y) - (1+\Delta)\frac{v^2(y)}{2}\right]_0^{v_{DS}}$$

or

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS} - (1+\Delta)\frac{v^2_{DS}}{2}\right]$$

To find $v_{DS}(sat)$, set the derivative of i_D with respect to v_{DS} equal to zero and solve for $v_{DS} = v_{DS}(sat)$ to get,

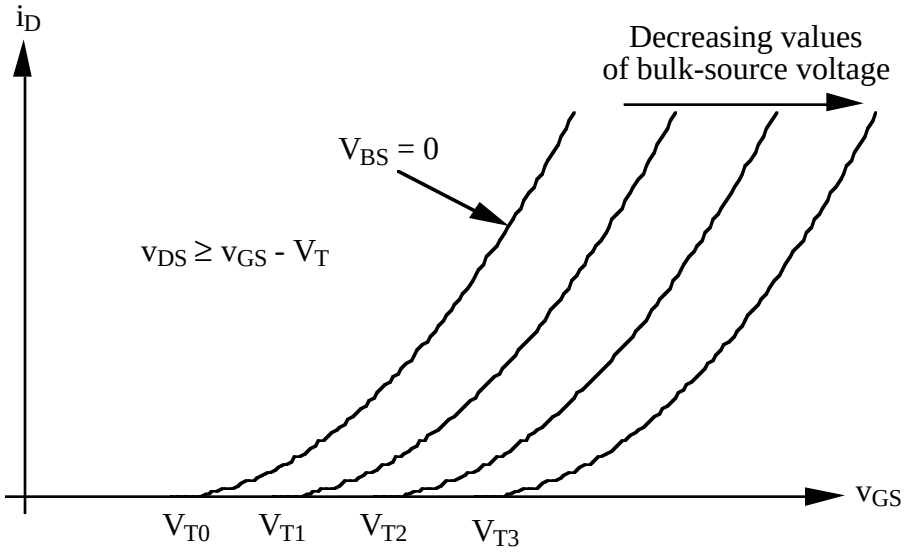
$$v_{DS}(sat) = \frac{v_{GS} - V_T}{1 + \Delta}$$

Therefore, in the saturation region, the drain current is

$$i_D = \frac{W\mu_o C_{ox}}{2(1+\Delta)L}\left(v_{GS} - V_T\right)^2$$

EFFECTS OF BACK GATE (BULK-SOURCE)

Bulk-Source (v_{BS}) influence on the transconductance characteristics-



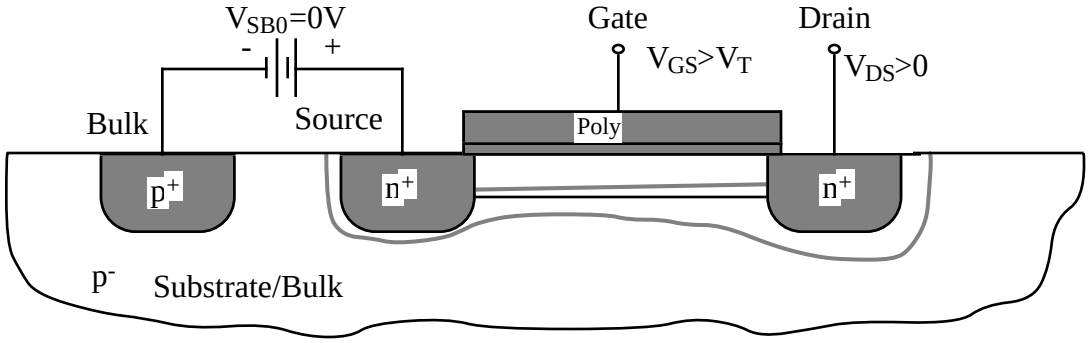
In general, the simple model incorporates the bulk effect into V_T by the following empirically developed equation-

$$V_{T(V_{BS})} = V_{T0} + \gamma\sqrt{2|\phi_f| + |v_{BS}|} - \gamma\sqrt{2|\phi_f|}$$

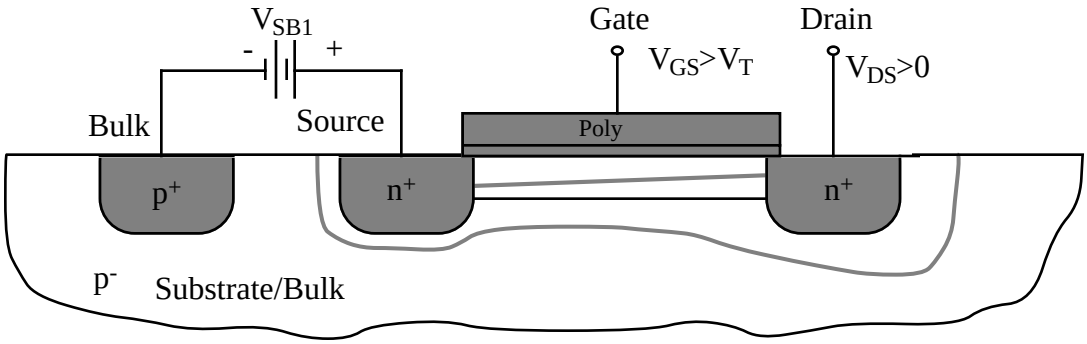
EFFECTS OF THE BACK GATE - CONTINUED

Illustration-

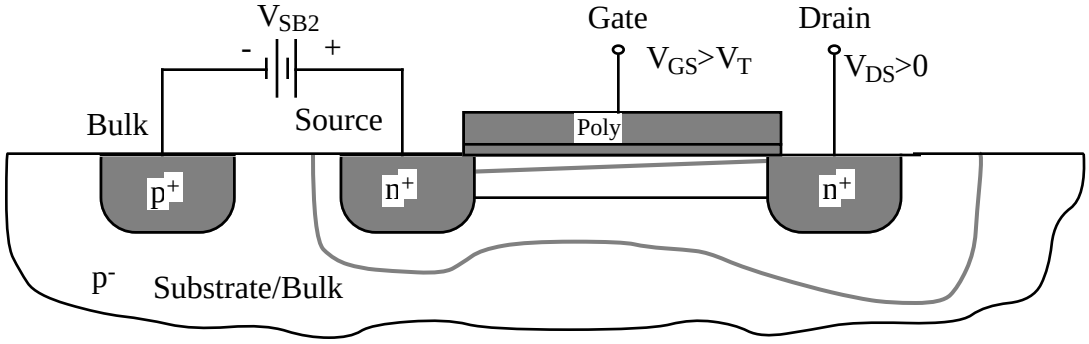
$V_{SB0} = 0V$:



$V_{SB1}>0V$:

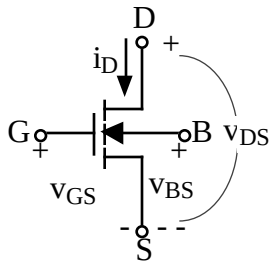


$V_{SB2} > V_{SB1}$:



SAH MODEL INCLUDING CHANNEL LENGTH MODULATION

N-channel reference convention:



Non-saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]$$

Saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS}(sat) - \frac{v_{DS}(sat)^2}{2}\right](1 + \lambda v_{DS})$$

$$= \frac{W\mu_o C_{ox}}{2L}(v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

where:

μ_o = zero field mobility (cm^2/volt·sec)

C_{ox} = gate oxide capacitance per unit area (F/cm^2)

λ = channel-length modulation parameter ($volts^{-1}$)

$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|}\right)$

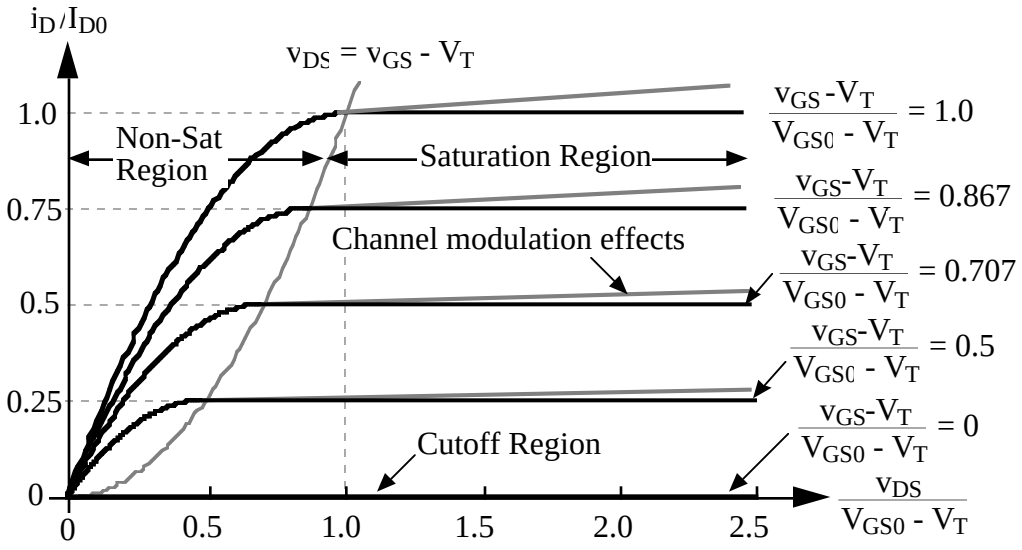
V_{T0} = zero bias threshold voltage

γ = bulk threshold parameter ($volts^{1/2}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

When solving for p-channel devices, negate all voltages and use the n-channel model with p-channel parameters and negate the current. Also negate V_{T0} of the p device.

OUTPUT CHARACTERISTICS OF THE MOS TRANSISTOR



Notation:

$$ß = K'\left(\frac{W}{L}\right) = (\mu_o C_{ox})\frac{W}{L}$$

Note:

$$\mu_o C_{ox} = K'$$

GRAPHICAL INTERPRETATION OF λ

Assume the MOS is transistor is saturated-

$$\therefore\ i_D = \frac{\mu C_{ox} W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

Define $i_D(0) = i_D$ when $v_{DS} = 0V$.

$$\therefore\ i_D(0) = \frac{\mu C_{ox} W}{2L}(v_{GS} - V_T)^2$$

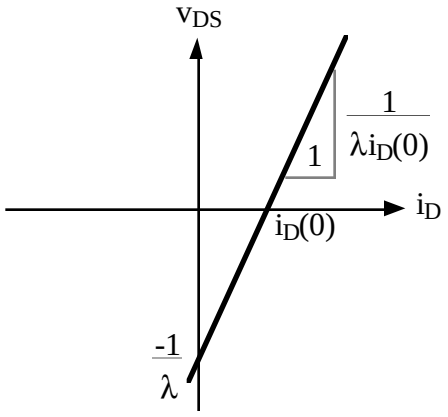
Now,

$$i_D = i_D(0)\,[1+\lambda v_{DS}] = i_D(0) + \lambda i_D(0)\, v_{DS}$$

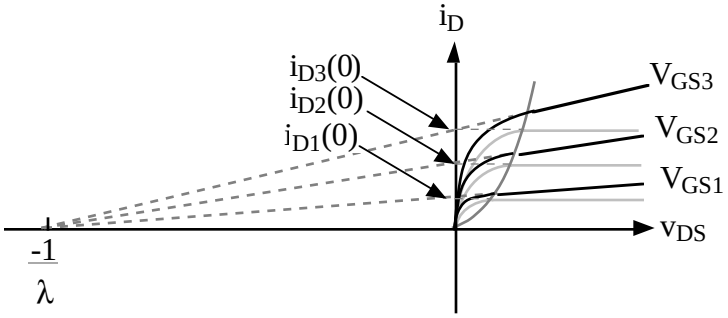
or

$$v_{DS} = \left[\frac{1}{\lambda i_D(0)}\right] i_D - \frac{1}{\lambda}$$

Matching with y = mx + b gives



or

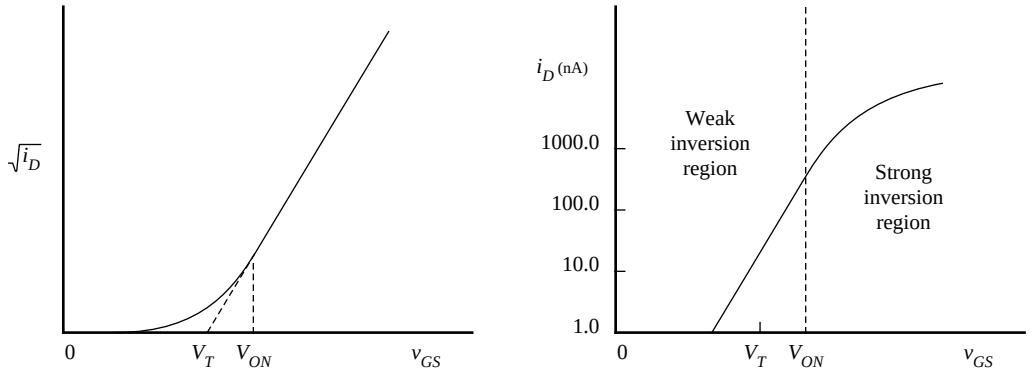


SPICE LEVEL 1 MODEL PARAMETERS FOR A TYPICAL BULK CMOS PROCESS (0.8μm)

Model Parameter	Parameter Description	Typical Parameter Value		Units
		NMOS	PMOS	
V_{T0}	Threshold Voltage for $V_{BS} = 0V$	0.75±0.15	−0.85±0.15	Volts
K'	Transconductance Parameter (sat.)	110±10%	50±10%	$\mu A/V^2$
γ	Bulk Threshold Parameter	0.4	0.57	$\sqrt{V}$
λ	Channel Length Modulation Parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	V^{-1}
$\phi = 2\phi_F$	Surface potential at strong inversion	0.7	0.8	Volts

These values are based on a 0.8 μm silicon-gate bulk CMOS n-well process.

WEAK INVERSION MODEL (Simple)



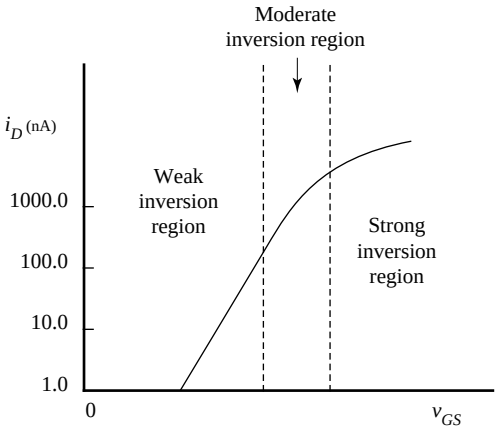
This model is appropriate for hand calculations but it does not accommodate a smooth transition into the strong-inversion region.

$$i_D \cong \frac{W}{L} I_{DO} \exp\left(\frac{q v_{GS}}{nkT}\right)$$

The transition point where this relationship is valid occurs at approximately

$$v_{gs} < V_T + n\frac{kT}{q}$$

<u>Weak-Moderate-Strong Inversion Approximation</u>



INTRINSIC CAPACITORS OF THE MOSFET

Types of MOS Capacitors

1. Depletion capacitance (C_{BD} and C_{BS})
2. Gate capacitances (C_{GS}, C_{GD}, and C_{GB})

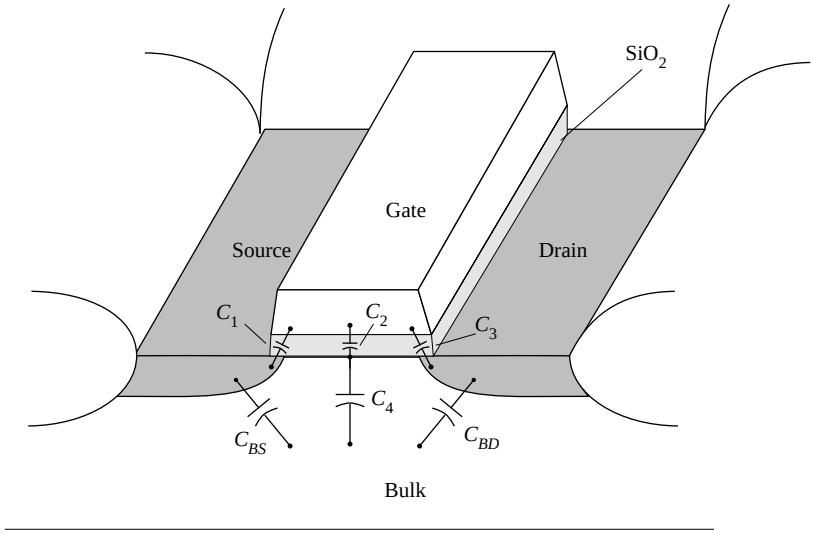
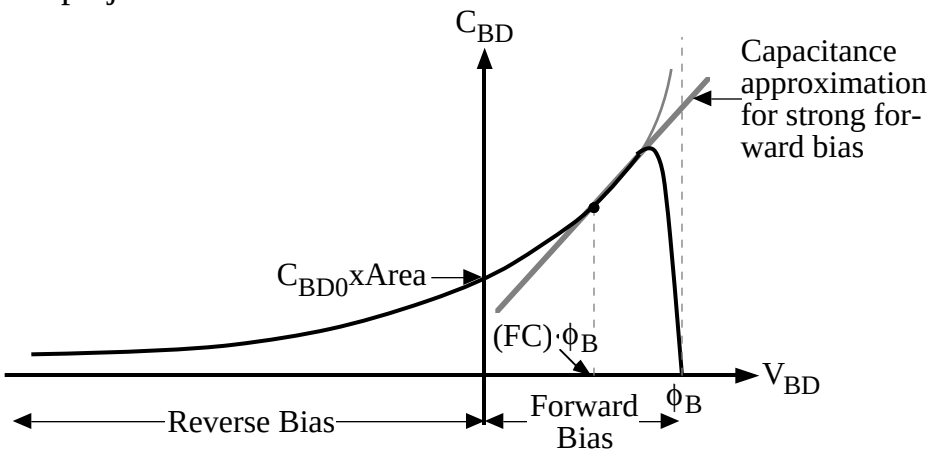


Figure 3.2-4 Large-signal, charge-storage capacitors of the MOS device.

Depletion Capacitors

Bulk-drain pn junction -



$$C_{BD} = \frac{C_{BD0}\,A_{BD}}{\left(1 - \frac{v_{BD}}{\phi_B}\right)^{MJ}} \quad \text{and} \quad C_{BS} = \frac{C_{BS0}\,A_{BS}}{\left(1 - \frac{v_{BS}}{\phi_B}\right)^{MJ}}$$

where,

A_{BD} (A_{BS}) = area of the bulk-drain (bulk-source)

ϕ_B = bulk junction potential (barrier potential)

MJ = bulk junction grading coefficient ($0.33 \le MJ \le 0.5$)

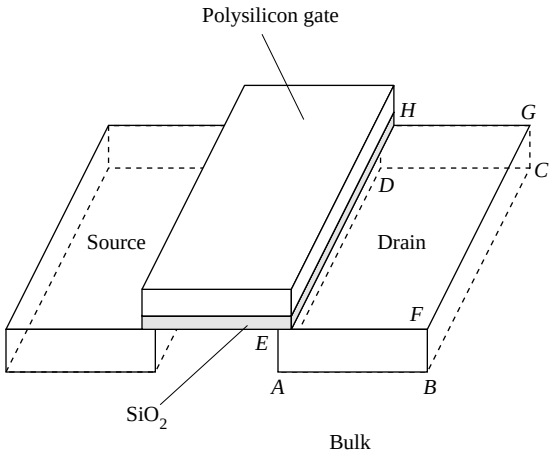
For strong forward bias, approximate the behavior by the tangent to the above C_{BD} or C_{BS} curve at v_{BD} or v_{BS} equal to $(FC)\cdot\phi_B$.

$$C_{BD} = \frac{C_{BD0}A_{BD}}{(1+FC)^{1+MJ}}\left[1 - (1+MJ)FC + FC\left(\frac{v_{BD}}{\phi_B}\right)\right], \quad v_{BD} > (FC)\cdot\phi_B$$

and

$$C_{BD} = \frac{C_{BS0}A_{BS}}{(1+FC)^{1+MJ}}\left[1 - (1+MJ)FC + FC\left(\frac{v_{BS}}{\phi_B}\right)\right], \quad v_{BS} > (FC)\cdot\phi_B$$

Bottom & Sidewall Approximations



Drain bottom = *ABCD*
Drain sidewall = *ABFE* + *BCGF* + *DCGH* + *ADHE*

$$C_{BX} = \frac{(CJ)(AX)}{\left[1 - \left(\frac{v_{BX}}{PB}\right)\right]^{MJ}} + \frac{(CJSW)(PX)}{\left[1 - \left(\frac{v_{BX}}{PB}\right)\right]^{MJSW}}, \quad v_{BX} \le (FC)(PB)$$

and

$$C_{BX} = \frac{(CJ)(AX)}{(1 - FC)^{1+MJ}} \left[1 - (1 + MJ)FC + MJ\,\frac{v_{BX}}{PB}\right]$$

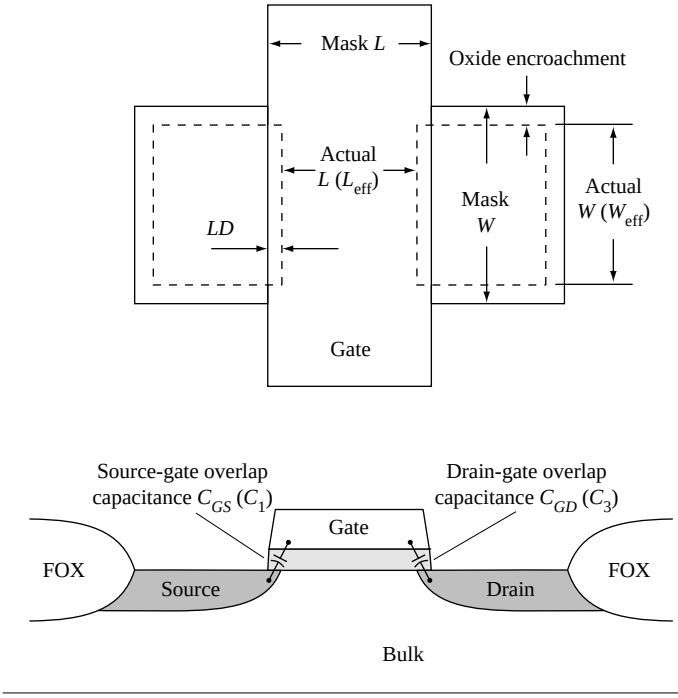
$$+ \frac{(CJSW)(PX)}{(1 - FC)^{1+MJSW}} \left[1 - (1 + MJSW)FC + \frac{v_{BX}}{PB}(MJSW)\right],$$

$$v_{BX} \ge (FC)(PB)$$

where

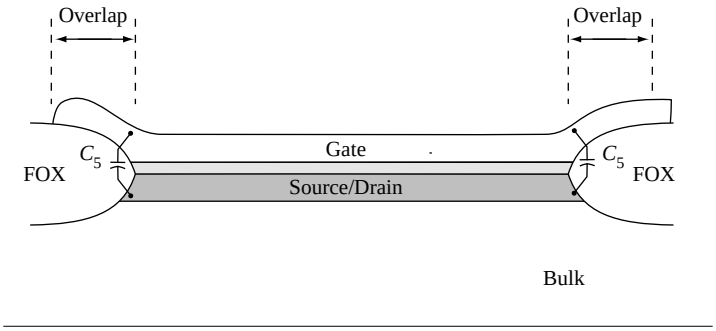
AX = area of the source (*X* = *S*) or drain (*X* = *D*)
PX = perimeter of the source (*X* = *S*) or drain (*X* = *D*)
CJSW = zero-bias, bulk-source/drain sidewall capacitance
MJSW = bulk-source/drain sidewall grading coefficient

Overlap Capacitance



$$C_1 = C_3 \cong (LD)(W_{\text{eff}})C_{ox} = (CGXO)W_{\text{eff}}$$

Gate to Bulk Overlap Capacitance



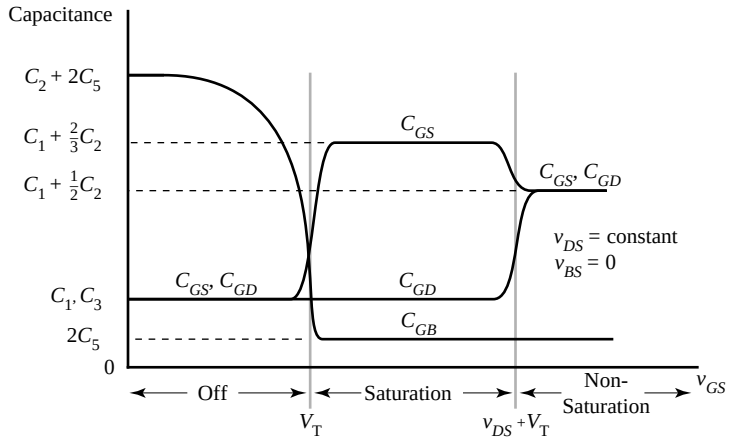
On a per-transistor basis, this is generally quite small

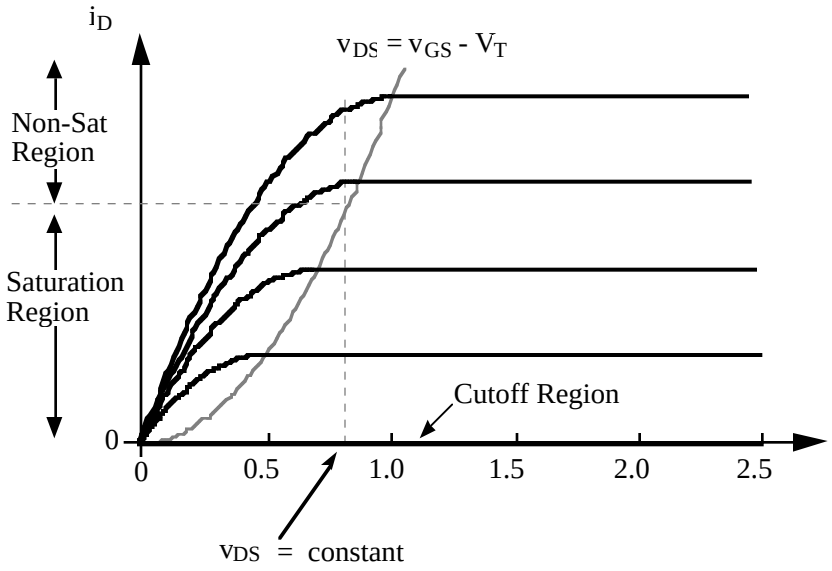
Channel Capacitance

$$C_2 = W_{\text{eff}}(L - 2LD)C_{ox} = W_{\text{eff}}(L_{\text{eff}})C_{ox}$$

Drain and source portions depend upon operating condition of transistor.

MOSFET Gate Capacitance Summary:





C_{GS}, C_{GD}, and C_{GB}

Off

$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{\text{eff}})(L_{\text{eff}}) + CGBO(L_{\text{eff}})$$

$$C_{GS} = C_1 \cong C_{ox}(LD)(W_{\text{eff}}) = CGSO(W_{\text{eff}})$$

$$C_{GD} = C_3 \cong C_{ox}(LD)(W_{\text{eff}}) = CGDO(W_{\text{eff}})$$

Saturation

$$C_{GB} = 2C_5 = CGBO\ (L_{\text{eff}})$$

$$C_{GS} = C_1 + (2/3)C_2 = C_{ox}(LD + 0.67L_{\text{eff}})(W_{\text{eff}})$$

$$= CGSO(W_{\text{eff}}) + 0.67C_{ox}(W_{\text{eff}})(L_{\text{eff}})$$

$$C_{GD} = C_3 \cong C_{ox}(LD)(W_{\text{eff}}) = CGDO(W_{\text{eff}})$$

Nonsaturated

$$C_{GB} = 2C_5 = CGBO\ (L_{\text{eff}})$$

$$C_{GS} = C_1 + 0.5C_2 = C_{ox}(LD + 0.5L_{\text{eff}})(W_{\text{eff}})$$

$$= (CGSO + 0.5C_{ox}L_{\text{eff}})W_{\text{eff}}$$

$$C_{GD} = C_3 + 0.5C_2 = C_{ox}(LD + 0.5L_{\text{eff}})(W_{\text{eff}})$$

$$= (CGDO + 0.5C_{ox}L_{\text{eff}})W_{\text{eff}}$$

Small-Signal Model for the MOS Transistor

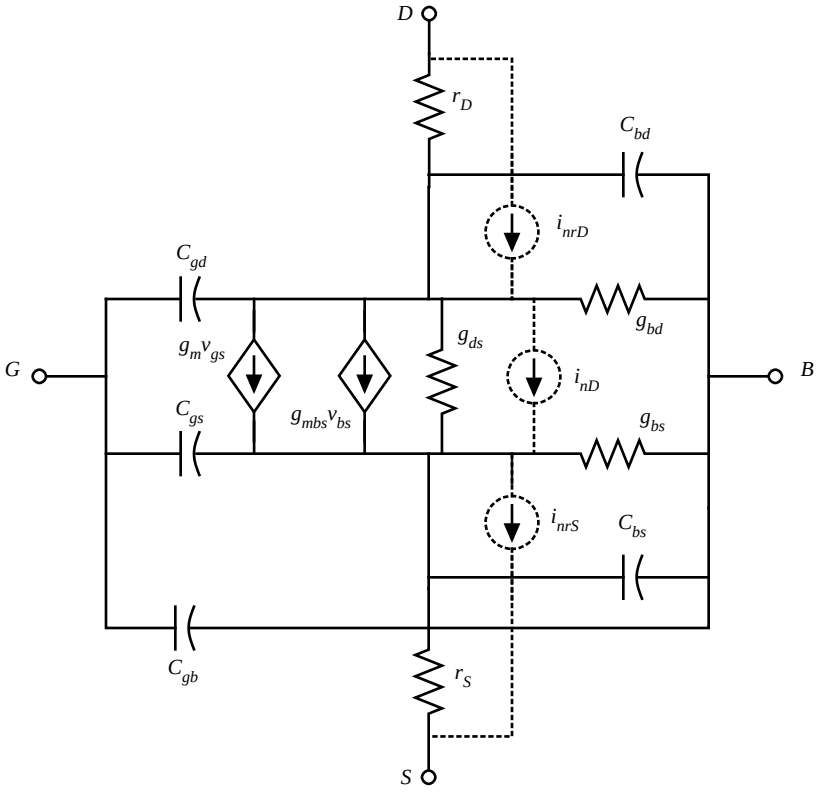


Figure 3.3-1 Small-signal model of the MOS transistor.

$$g_{bd} = \frac{\partial I_{BD}}{\partial V_{BD}} \text{(at the quiescent point)} \cong 0$$

and

$$g_{bs} = \frac{\partial I_{BS}}{\partial V_{BS}} \text{(at the quiescent point)} \cong 0$$

The channel conductances, g_m, g_{mbs}, and g_{ds} are defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{(at the quiescent point)}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} \text{(at the quiescent point)}$$

and

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \text{(at the quiescent point)}$$

Saturation Region

$$g_m = \sqrt{(2K'W/L)|I_D|(1+\lambda V_{DS})} \cong \sqrt{(2K'W/L)|I_D|}$$

$$g_{mbs} = \frac{-\partial I_D}{\partial V_{SB}} = -\left(\frac{\partial I_D}{\partial V_T}\right)\left(\frac{\partial V_T}{\partial V_{SB}}\right)$$

Noting that $\frac{\partial I_D}{\partial V_T} = \frac{-\partial I_D}{\partial V_{GS}}$, we get

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = \eta\, g_m$$

$$g_{ds} = g_o = \frac{I_D \lambda}{1 + \lambda V_{DS}} \cong I_D \lambda$$

Relationships of the Small Signal Model Parameters upon the DC Values of Voltage and Current in the Saturation Region.

Small Signal Model Parameters	DC Current	DC Current and Voltage	DC Voltage
g_m	$\cong (2K' I_D W/L)^{1/2}$	–	$\cong \frac{2K' W}{L}(V_{GS} - V_T)$
g_{mbs}	—	$\frac{\gamma (2I_D\beta)^{1/2}}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$	$\frac{\gamma(\beta(V_{GS} - V_T))}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$
g_{ds}	$\cong \lambda I_D$	—	—

Nonsaturation region

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = \beta V_{DS}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\beta\gamma V_{DS}}{2(2|\phi_F| + V_{SB})^{1/2}}$$

and

$$g_{ds} = \beta(V_{GS} - V_T - V_{DS})$$

Relationships of the Small-Signal Model Parameters upon the DC Values of Voltage and Current in the Nonsaturation Region.

Small Signal Model Parameters	DC Voltage and/or Current Dependence
g_m	$= \beta V_{DS}$
g_{mbs}	$\frac{\beta \gamma V_{DS}}{2(2\|\phi_F\| + V_{SB})^{1/2}}$
g_{ds}	$= \beta (V_{GS} - V_T - V_{DS})$

Noise

$$\overline{i}^2_{nrD} = \left(\frac{4kT}{r_D}\right)\Delta f \quad (A^2)$$

$$\overline{i}^2_{nrS} = \left(\frac{4kT}{r_S}\right)\Delta f \quad (A^2)$$

and

$$\overline{i}^2_{nD} = \left[\frac{8kT\, g_m(1+\eta)}{3} + \frac{(KF)I_D}{f\, C_{ox}\, L^2}\right]\Delta f \quad (A^2)$$

SPICE Level 3 Model

The large-signal model of the MOS device previously discussed neglects many important second-order effects. Most of these second-order effects are due to narrow or short channel dimensions (less than about 3μm). We shall also consider the effects of temperature upon the parameters of the MOS large signal model.
We first consider second-order effects due to small geometries. When v_{GS} is greater than V_T, the drain current for a small device can be given as

Drain Current

$$i_{DS} = \text{BETA}\left[v_{GS} - V_T - \left(\frac{1+f_b}{2}\right)v_{DE}\right]\cdot v_{DE} \tag{1}$$

$$\text{BETA} = \text{KP}\,\frac{W_{\text{eff}}}{L_{\text{eff}}} = \mu_{\text{eff}}\text{COX}\,\frac{W_{\text{eff}}}{L_{\text{eff}}} \tag{2}$$

$$L_{\text{eff}} = L - 2(\text{LD}) \tag{3}$$

$$W_{\text{eff}} = W - 2(\text{WD}) \tag{4}$$

$$v_{DE} = \min(v_{DS}\,,\, v_{DS}\,(\text{sat})) \tag{5}$$

$$f_b = f_n + \frac{\text{GAMMA}\cdot f_s}{4(\text{PHI} + v_{SB})^{1/2}} \tag{6}$$

Note that PHI is the SPICE model term for the quantity $2\phi_f$. Also be aware that PHI is always positive in SPICE regardless of the transistor type (p- or n-channel).

$$f_n = \frac{\text{DELTA}}{W_{\text{eff}}}\frac{\pi\varepsilon_{\text{si}}}{2\cdot\text{COX}} \tag{7}$$

$$f_s = 1 - \frac{x_j}{L_{\text{eff}}}\left\{\frac{\text{LD}+wc}{x_j}\left[1-\left(\frac{wp}{x_j+wp}\right)^2\right]^{1/2} - \frac{\text{LD}}{x_j}\right\} \tag{8}$$

$$wp = xd\,(\text{PHI} + v_{SB}\,)^{1/2} \tag{9}$$

$$xd = \left(\frac{2\cdot\varepsilon_{si}}{q\cdot\text{NSUB}}\right)^{1/2} \tag{10}$$

$$wc = x_j\left[k_1 + k_2\left(\frac{wp}{x_j}\right) - k_3\left(\frac{wp}{x_j}\right)^2\right] \tag{11}$$

$k_1 = 0.0631353$, $k_2 = 0.08013292$, $k_3 = 0.01110777$

Threshold Voltage

$$V_T = V_{bi} - \left(\frac{\text{ETA}\cdot 8.15^{-22}}{C_{\text{ox}}\, L_{\text{eff}}^3}\right)v_{DS} + \text{GAMMA}\cdot f_s(\text{PHI} + v_{SB})^{1/2} + f_n(\text{PHI} + v_{SB}) \tag{12}$$

$$v_{bi} = \text{v}_{fb} + \text{PHI} \tag{13}$$

or

$$v_{bi} = \text{VTO} - \text{GAMMA}\cdot\sqrt{\text{PHI}} \tag{14}$$

Saturation Voltage

$$v_{sat} = \frac{v_{gs} - V_T}{1 + f_b} \tag{15}$$

$$v_{DS}(\text{sat}) = v_{sat} + v_C - \left(v_{\text{sat}}^2 + v_C^2\right)^{1/2} \tag{16}$$

$$v_C = \frac{\text{VMAX}\cdot L_{\text{eff}}}{\mu_{\text{s}}} \tag{17}$$

If VMAX is not given, then $v_{DS}(\text{sat}) = v_{sat}$

Effective Mobility

$$\mu_s = \frac{\text{U0}}{1 + \text{THETA}\,(v_{GS} - V_T)} \text{ when VMAX = 0} \tag{18}$$

$$\mu_{\text{eff}} = \frac{\mu_s}{1 + \dfrac{v_{DE}}{v_C}} \text{ when VMAX > 0; otherwise } \mu_{\text{eff}} = \mu_s \tag{19}$$

Channel-Length Modulation

When VMAX = 0

$$\Delta L = xd\left[\text{KAPPA}\ (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{20}$$

when VMAX > 0

$$\Delta L = -\frac{ep \cdot xd^2}{2} + \left[\left(\frac{ep \cdot xd^2}{2}\right)^2 + \text{KAPPA} \cdot xd^2 \cdot (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{21}$$

where

$$ep = \frac{v_C\,(v_C + v_{DS}(\text{sat}))}{L_{\text{eff}}\, v_{DS}\,(\text{sat})} \tag{22}$$

$$i_{DS} = \frac{i_{DS}}{1 - \Delta L} \tag{21}$$

Weak Inversion Model (Level 3)

In the SPICE Level 3 model, the transition point from the region of strong inversion to the weak inversion characteristic of the MOS device is designated as v_{on} and is greater than V_T. v_{on} is given by

$$v_{on} = V_T + fast \tag{1}$$

where

$$fast = \frac{kT}{q}\left[1 + \frac{q \cdot NFS}{\text{COX}} + \frac{\text{GAMMA} \cdot f_s\,(\text{PHI} + v_{SB})^{1/2} + f_n\,(\text{PHI} + v_{SB})}{2(\text{PHI} + v_{SB})}\right] \tag{2}$$

NFS is a parameter used in the evaluation of v_{on} and can be extracted from measurements. The drain current in the weak inversion region, v_{GS} less than v_{on}, is given as

$$i_{DS} = i_{DS}\,(v_{on}, v_{DE}, v_{SB})\, e^{\left(\frac{v_{GS} - v_{on}}{fast}\right)} \tag{3}$$

where i_{DS} is given as (from Eq. (1), Sec. 3.4 with v_{GS} replaced with v_{on})

$$i_{DS} = \text{BETA}\left[v_{on} - V_T - \left(\frac{1 + f_b}{2}\right)v_{DE}\right] \cdot v_{DE} \tag{4}$$

Typical Model Parameters Suitable for SPICE Simulations Using Level-3 Model (Extended Model). These Values Are Based upon a 0.8μm Si-Gate Bulk CMOS n-Well Process

Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	P-Channel	Units
VTO	Threshold	0.7 ± 0.15	-0.7 ± 0.15	V
UO	mobility	660	210	$cm^2/V\text{-}s$
DELTA	Narrow-width threshold adjust factor	2.4	1.25	—
ETA	Static-feedback threshold adjust factor	0.1	0.1	—
KAPPA	Saturation field factor in channel-length modulation	0.15	2.5	1/V
THETA	Mobility degradation factor	0.1	0.1	1/V
NSUB	Substrate doping	3×10^{16}	6×10^{16}	cm^{-3}
TOX	Oxide thickness	140	140	Å
XJ	Mettallurgical junction depth	0.2	0.2	μm
WD	Delta width			μm
LD	Lateral diffusion	0.016	0.015	μm
NFS	Parameter for weak inversion modeling	7×10^{11}	6×10^{11}	cm^{-2}
CGSO		220×10^{-12}	220×10^{-12}	F/m
CGDO		220×10^{-12}	220×10^{-12}	F/m
CGBO		700×10^{-12}	700×10^{-12}	F/m
CJ		770×10^{-6}	560×10^{-6}	F/m^2
CJSW		380×10^{-12}	350×10^{-12}	F/m
MJ		0.5	0.5	
MJSW		0.38	0.35	
NFS	Parameter for weak inversion modeling	7×10^{11}	6×10^{11}	cm^{-2}

Temperature Dependence

The temperature-dependent variables in the models developed so far include the: Fermi potential, PHI, EG, bulk junction potential of the source-bulk and drain-bulk junctions, PB, the reverse currents of the pn junctions, I_S, and the dependence of mobility upon temperature. The temperature dependence of most of these variables is found in the equations given previously or from well-known expressions. The dependence of mobility upon temperature is given as

$$\mathrm{UO}(T) = \mathrm{UO}(T_0)\left(\frac{T}{T_0}\right)^{\mathrm{BEX}}$$

where BEX is the temperature exponent for mobility and is typically -1.5.

$$v_{therm}(T) = \frac{KT}{q}$$

$$\mathrm{EG}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \left[\frac{T^2}{T + 1108.0}\right]$$

$$\mathrm{PHI}(T) = \mathrm{PHI}(T_0) \cdot \left(\frac{T}{T_0}\right) - v_{therm}(T)\left[3 \cdot \ln\left(\frac{T}{T_0}\right) + \frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)}\right]$$

$$v_{bi}(T) = v_{bi}(T_0) + \frac{\mathrm{PHI}(T) - \mathrm{PHI}(T_0)}{2} + \frac{\mathrm{EG}(T_0) - \mathrm{EG}(T)}{2}$$

$$\mathrm{VT0}(T) = v_{bi}(T) + \mathrm{GAMMA}\left[\sqrt{\mathrm{PHI}(T)}\right]$$

$$\mathrm{PHI}(T) = 2 \cdot v_{therm} \ln\left(\frac{\mathrm{NSUB}}{n_i(T)}\right)$$

$$n_{i(T)} = 1.45 \cdot 10^{16} \cdot \left(\frac{T}{T_0}\right)^{3/2} \cdot \exp\left[\mathrm{EG} \cdot \left(\frac{T}{T_0} - 1\right) \cdot \left(\frac{1}{2 \cdot v_{therm}(T_0)}\right)\right]$$

For drain and source junction diodes, the following relationships apply.

$$\mathrm{PB}(T) = \mathrm{PB} \cdot \left(\frac{T}{T_0}\right) - v_{therm}(T)\left[3 \cdot \ln\left(\frac{T}{T_0}\right) + \frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)}\right]$$

$$I_S(T) = \frac{I_S(T_0)}{\mathrm{N}} \cdot \exp\left[\frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)} + 3 \cdot \ln\left(\frac{T}{T_0}\right)\right]$$

where N is diode emission coefficient. The nominal temperature, T_0, is 300 K.

SPICE Simulation of MOS Circuits

Minimum required terms for a transistor instance follows:

M1 3 6 7 0 NCH W=100U L=1U

"M," tells SPICE that the instance is an MOS transistor (just like "R" tells SPICE that an instance is a resistor). The "1" makes this instance unique (different from M2, M99, etc.)

The four numbers following"M1" specify the nets (or nodes) to which the drain, gate, source, and substrate (bulk) are connected. These nets have a specific order as indicated below:

M<number> <DRAIN> <GATE> <SOURCE> <BULK> ...

Following the net numbers, is the model name governing the character of the particular instance. In the example given above, the model name is "NCH." There must be a model description of "NCH."

The transistor width and length are specified for the instance by the "W=100U" and "L=1U" expressions.

The default units for width and length are meters so the "U" following the number 100 is a multiplier of 10^{-6}. [Recall that the following multipliers can be used in SPICE: M, U, N, P, F, for 10^{-3}, 10^{-6}, 10^{-9}, 10^{-12} , 10^{-15} , respectively.]

Additional information can be specified for each instance. Some of these are

Drain area and periphery (AD and PD) ← calc depl cap and leakage
Source area and periphery (AS and PS) ← calc depl cap and leakage
Drain and source resistance in squares (NRD and NRS)
Multiplier designating how many devices are in parallel (M)
Initial conditions (for initial transient analysis)

The number of squares of resistance in the drain and source (NRD and NRS) are used to calculate the drain and source resistance for the transistor.

Geometric Multiplier: M

To apply the “unit-matching” principle, use the geometric multiplier feature rather than scale W/L.

This:

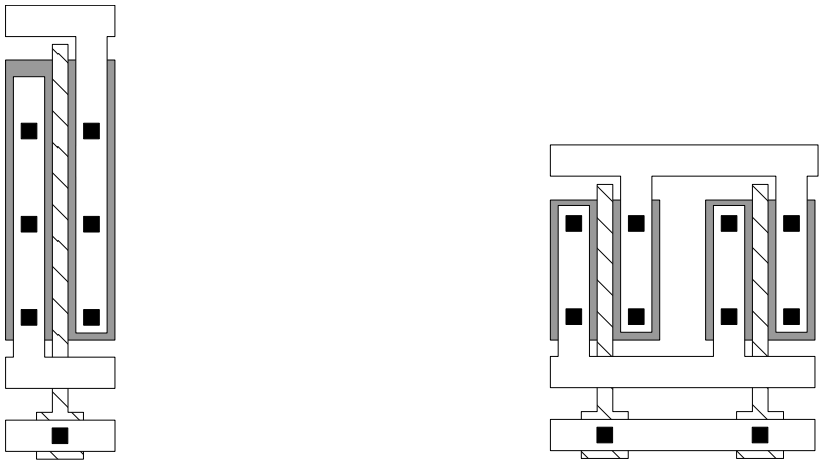
```
M1 3 2 1 0 NCH W=20U L=1U
```

is not the same as this:

```
M1 3 2 1 0 NCH W=10U L=1U M=2
```

The following dual instantiation is equivalent to using a multiplier

```
M1A 3 2 1 0 NCH W=10U L=1U
M1B 3 2 1 0 NCH W=10U L=1U
```



(a) (b)

(a)M1 3 2 1 0 NCH W=20U L=1U. (b) M1 3 2 1 0 NCH W=10U L=1U M=1.
.

MODEL Description

A SPICE simulation file for an MOS circuit is incomplete without a description of the model to be used to characterize the MOS transistors used in the circuit. A model is described by placing a line in the simulation file using the following format.

```
.MODEL <MODEL NAME> <MODEL TYPE> <MODEL PARAMETERS>
```

MODEL NAME e.g., "NCH"
MODEL TYPE either "PMOS" or "NMOS."

MODEL PARAMETERS :

```
LEVEL=1 VTO=1 KP=50U GAMMA=0.5 LAMBDA=0.01
```

SPICE can calculate what you do not specify

You must specify the following

- surface state density, NSS, in cm^{-2}
- oxide thickness, TOX, in meters
- surface mobility, UO, in $cm^2/V\text{-}s$,
- substrate doping, NSUB, in cm^{-3}

The equations used to calculate the electrical parameters are

$$\text{VTO} = \phi_{MS} - \frac{q(\text{NSS})}{(\varepsilon_{ox}/\text{TOX})} + \frac{(2q \cdot \varepsilon_{si} \cdot \text{NSUB} \cdot \text{PHI})^{1/2}}{(\varepsilon_{ox}/\text{TOX})} + \text{PHI}$$

$$\text{KP} = \text{UO}\,\frac{\varepsilon_{ox}}{\text{TOX}}$$

$$\text{GAMMA} = \frac{(2q \cdot \varepsilon_{si} \cdot \text{NSUB})^{1/2}}{(\varepsilon_{ox}/\text{TOX})}$$

and

$$\text{PHI} = \left| 2\phi_F \right| = \frac{2kT}{q} \ln\left(\frac{\text{NSUB}}{n_i}\right)$$

LAMBDA is not calculated from the process parameters for the LEVEL 1 model.

Other parameters:

IS: Reverse current of the drain-bulk or source-bulk junctions in Amps

JS: Reverse-current density in A/m^2

JS requires the specification of AS and AD on the model line. If IS is specified, it overrides JS. The default value of IS is usually 10^{-14} A.

RD: Drain ohmic resistance in ohms

RS: Source ohmic resistance in ohms

RSH: Sheet resistance in ohms/square. RSH is overridden if RD or RS are entered. To use RSH, the values of NRD and NRS must be entered on the model line.

The drain-bulk and source-bulk depletion capacitors

CJ: Bulk bottom plate junction capacitance
MJ: Bottom plate junction grading coefficient
CJSW: Bulk sidewall junction capacitance
MJSW: Sidewall junction grading coefficient

If CJ is entered as a model parameter it overrides the calculation of CJ using NSUB, otherwise, CJ is calculated using NSUB.

If CBD and CBS are entered, these values override CJ and NSUB calculations.

In order for CJ to result in an actual circuit capacitance, the transistor instance must include AD and AS.

In order for CJSW to result in an actual circuit capacitance, the transistor instance must include PD and PS.

CGSO: Gate-Source overlap capacitance (at zero bias)
CGDO: Gate-Drain overlap capacitance (at zero bias)

AF: Flicker noise exponent
KF: Flicker noise coefficient

TPG: Indicates type of gate material relative to the substrate

TPG=1 > gate material is opposite of the substrate
TPG=-1 > gate material is the same as the substrate
TPG=0 > gate material is aluminum

XQC: Channel charge flag and fraction of channel charge attributed to the drain