

Homework 3**1) CMOS Inverter**

- a) Use HSpice to plot the transfer characteristics (output vs. input) of a CMOS inverter with $(W/L)_n=2.4\mu\text{m}/1.2\mu\text{m}$ and $(W/L)_p=6.0\mu\text{m}/1.2\mu\text{m}$, respectively. Simulate your circuit for the two bipolar supply voltages of $\pm 1.5\text{V}$ and $\pm 2.5\text{V}$. For each case, deduce the voltage gain and the approximate linear output range.
- b) Compute the voltage gain from a linear equivalent circuit and compare your results with the values deduced from HSpice simulations.
- c) Load the inverter with a capacitor of 100 fF and simulate its response to a symmetrical pulsed input voltage with rail-to-rail voltage swing, a period of 50 ns and rise and fall times of 0.5 ns. Run your simulations for both $\pm 1.5\text{V}$ and $\pm 2.5\text{V}$ supply rails and find the corresponding 10-90% rise and fall times of the output voltage.
- d) Repeat the above simulations for an inverter with $(W/L)_n=1.2\mu\text{m}/0.6\mu\text{m}$ and $(W/L)_p=3.0\mu\text{m}/0.6\mu\text{m}$. Explain the differences.

2) Common-Drain Amplifier (Source Follower)

Design a common-drain amplifier that keeps the voltage gain close to unity and yields an output resistance of less than 5 k Ω . Use a p-channel device as the active gain stage and establish the Q-point current I_{DQ} by means of a current source. The latter will also be realized by a p-channel device. The supply rails are $\pm 2.5\text{V}$.

- a) Find the relationship between output resistance r_{out} and bias current I_{DQ} .
- b) Assume that the p-channel output stage features a (W/L) ratio of $30\mu\text{m}/1.2\mu\text{m}$. What is the minimum value of the bias current I_{DQ} that guarantees r_{out} to be less than 5 k Ω ?
- c) Compute the voltage gain in the absence of a body effect.
- d) How much voltage gain is lost (in %) if you include the body effect?
- e) Apply a sinusoidal input voltage of 1 V and use HSpice to confirm your theoretical results.
- f) What is the maximum input voltage swing (peak-to-peak) your circuit can accommodate? Define the swing limit as the voltage that causes a total harmonic distortion in excess of 1%. Use HSpice to find the answer and analyze the circuit both with and without a body effect.

SPICE BSIM3 VERSION 3.1 PARAMETERS

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.MODEL nfet NMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 49
+XJ = 1.5E-7           NCH = 1.7E17       TOX = 1.39E-8
+K1 = 0.8857752       K2 = -0.0935679    VTH0 = 0.6398186
+K3B = -7.6711263     W0 = 1E-8          K3 = 22.1010569
+DVT0W = 0            DVT1W = 0          NLX = 1E-9
+DVT0 = 2.7950058     DVT1 = 0.4085592  DVT2W = 0
+UO = 453.2010286     UA = 2.494433E-13 DVT2 = -0.1237812
+UC = 2.022743E-11    VSAT = 1.730467E5  UB = 1.488658E-18
+AGS = 0.1151449     B0 = 2.792031E-6  A0 = 0.5543744
+KETA = -1.371458E-3  A1 = 0             B1 = 5E-6
+RDSW = 1.319508E3    PRWG = 0.0381943  A2 = 0.3560219
+WR = 1               WINT = 2.507126E-7 PRWB = 0.0141195
+XL = 0              XW = 0             LINT = 2.304464E-8
+DWB = 4.946821E-8    VOFF = 0           DWG = -1.755808E-8
+CIT = 0              CDSC = 2.4E-4      NFACTOR = 0.7910748
+CDSCB = 0            ETA0 = 0.0051332  CDSCD = 0
+DSUB = 0.1945608     PCLM = 2.253484   ETAB = -1.252309E-3
+PDIBLC2 = 2.440187E-3 PDIBLCB = -0.1294159 PDIBLC1 = -1
+PSCBE1 = 5.348212E8  PSCBE2 = 3.233314E-5 DROUT = 0.6751288
+DELTA = 0.01         RSH = 80.3         PVAG = 0
+PRT = 0              UTE = -1.5         MOBMOD = 1
+KT1L = 0             KT2 = 0.022        KT1 = -0.11
+UB1 = -7.61E-18     UC1 = -5.6E-11    UA1 = 4.31E-9
+WL = 0               WLN = 1            AT = 3.3E4
+WWN = 1              WWL = 0            WW = 0
+LLN = 1              LW = 0             LL = 0
+LWL = 0              CAPMOD = 2         LWN = 1
+CGDO = 2.12E-10     CGSO = 2.12E-10   XPART = 0.5
+CJ = 4.279445E-4     PB = 0.9616445    CGBO = 1E-9
+CJSW = 3.492439E-10 PBSW = 0.1         MJ = 0.4374524
+CJSWG = 1.64E-10    PBSWG = 0.1        MJSW = 0.1245165
+CF = 0               PVTH0 = 0.0431719 MJSWG = 0.1245165
+PK2 = -0.0350028    WKETA = -0.0230093 PRDSW = -30.376525
*                    LKETA = 2.090253E-3)

.MODEL pfet PMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 49
+XJ = 1.5E-7           NCH = 1.7E17       TOX = 1.39E-8
+K1 = 0.5429357       K2 = 9.433657E-3   VTH0 = -0.9488171
+K3B = -0.8567156     W0 = 1E-8          K3 = 3.2656684
+DVT0W = 0            DVT1W = 0          NLX = 1.48542E-8
+DVT0 = 2.530444      DVT1 = 0.5291909  DVT2W = 0
+UO = 220.9301068     UA = 3.049951E-9  DVT2 = -0.1040273
+UC = -5.63429E-11    VSAT = 2E5         UB = 1E-21
+AGS = 0.1506017     B0 = 9.121548E-7  A0 = 0.9085767
+KETA = -2.819843E-3  A1 = 0             B1 = 5E-6
+RDSW = 3E3           PRWG = -0.0464229  A2 = 0.3
+WR = 1               WINT = 2.90101E-7 PRWB = -0.0398483
+XL = 0              XW = 0             LINT = 4.254314E-8
+DWB = 1.788287E-8    VOFF = -0.0659109 DWG = -2.169468E-8
+CIT = 0              CDSC = 2.4E-4      NFACTOR = 0.8188201
+CDSCB = 0            ETA0 = 1.380153E-3 CDSCD = 0
+DSUB = 0.7658995     PCLM = 2.0797597  ETAB = -0.0429727
+PDIBLC2 = 4.521707E-3 PDIBLCB = -0.0437905 PDIBLC1 = 0.1113965
+PSCBE1 = 1.25116E10  PSCBE2 = 1.227353E-9 DROUT = 0.3065171
+DELTA = 0.01         RSH = 104.9       PVAG = 8.477076E-6
+PRT = 0              UTE = -1.5         MOBMOD = 1
+KT1L = 0             KT2 = 0.022        KT1 = -0.11
+UB1 = -7.61E-18     UC1 = -5.6E-11    UA1 = 4.31E-9
+WL = 0               WLN = 1            AT = 3.3E4
+WWN = 1              WWL = 0            WW = 0
+LLN = 1              LW = 0             LL = 0
+LWL = 0              CAPMOD = 2         LWN = 1
+CGDO = 2.25E-10     CGSO = 2.25E-10   XPART = 0.5
+CJ = 7.308538E-4     PB = 0.9416073    CGBO = 1E-9
+CJSW = 2.852637E-10 PBSW = 0.99        MJ = 0.4948413
+CJSWG = 6.4E-11     PBSWG = 0.99       MJSW = 0.3001719
+CF = 0               PVTH0 = 5.98016E-3 MJSWG = 0.3001719
+PK2 = 3.73981E-3    WKETA = 4.127712E-3 PRDSW = 14.8598424
*                    LKETA = -2.567864E-3)

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