

University of Rhode Island
ELE548: Computer Architecture
Fall 2008

Instructor: Resit Sendag
Office: Kelley Annex 219
Office Hours: MW 12:00-1:00pm or by appointment
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Class web page: <http://www.ele.uri.edu/faculty/sendag/ele548>

Time and Location: 5:00pm – 6:45pm, MW, Kelley Hall 203.

Credits: 4

Prerequisite: ELE 305 (Introduction to Computer Architecture) or ELE 405 (Digital Computer Design) or equivalent or permission of instructor

Required Text: *Computer Architecture: A Quantitative Approach (4th Edition)*, John Hennessy and David Patterson, Morgan Kaufmann Publishers, 2007.

Supplemental Text: *Modern Processor Design: Fundamentals of Superscalar Processors*, John Shen and Mikko Lipasti, McGraw-Hill, 2003.

The required text is available at the bookstore in memorial Union, and both books are available through Amazon.com.

Course Objective:

The goal of this course is to impart a deep understanding of high-performance computer system architecture. The emphasis is on pipelining, instruction level parallelism, memory hierarchy, storage systems, interconnection networks, and multi-processor design. Topics covered include branch prediction techniques, dynamic instruction scheduling, cache memory, main memory, virtual memory, I/O systems, buses, multistage interconnection networks, memory consistency models, synchronization, and cache coherence protocols. Term project aims to develop an understanding of the techniques for quantitative analysis and evaluation of modern computing systems, such as the selection of appropriate benchmarks to reveal and compare the performance of alternative design choices in system design. The course is intended for graduate students in electrical and computer engineering, and computer science.

Grading:

Homework Assignment:	20%	(4 assignments)
Midterm Exam:	30%	(in class)
Term Project:	50%	(meet with instructor every two weeks)

Important Dates:	Term Project proposal due:	October 1, 2008
	Term Project progress report due:	November 3, 2008
	Midterm exam:	November 19, 2008
	Term Project preliminary report due:	December 1, 2008
	Term Project final report due:	December 10, 2008

Computer Accounts:

If you don't already have one, you must get an *ELE account* to use the machines in Graduate Student Lab. You must contact the ELE System Manager for the account in Kelley 117. A storage area is granted for each ELE account designated as the folder */grads/account*. So if the login being used is *yourname*, the storage location for this user is */grads/yourname*. You will automatically get an email account: *yourname@ele.uri.edu*.

Term Project:

The best way to learn is by doing, and this project gives students a great opportunity to conduct experiments in computer architecture or explore more "far out" ideas. The intent of the project is to go through the research process and produce a research paper. A significant portion of your grade in this course will come from your final project instead of a final exam. This project will involve investigating some aspect of high-performance microprocessor architecture via simulation. Typically, a project investigates one of the areas discussed during class; however, you are free to propose any topic in microprocessor architecture. Your simulation study can be one of the two following types:

1. Propose some new architectural idea and quantitatively evaluate it using a simulation study.
2. Verify the results of a previously published research paper. For instance, you could determine the maximum amount of instruction-level parallelism (ILP) in a set of standard benchmark programs and compare your results to other ILP-limit studies; you could verify the properties of different types of branch predictors; you could determine how well a victim cache really works; etc.

The detailed information about the project and deliverables can be found in the attached "Project Requirements".

Expected Course Outline

Week	Dates	Topic	Reading	Due (except homework)
1	9/3	Meet with the class		
2	9/8 9/10	Introduction/Trends Review of pipelining	Ch1 App A	
3	9/15 9/17	ILP and dynamic execution //	Ch 2 & Ch3 //	

4	9/22 9/24	// //	// //	
5	9/29 10/1	// //	// //	Proj. Proposal
6	10/6 10/8	// Static Scheduling	// //	
7	10/13 10/15	Columbus Day //	NO CLASS //	
8	10/20 10/22	// Memory Systems	// Appendix C & Chapter 5	
9	10/27 10/29	// //	// //	
10	11/3 11/5	// //	// //	Proj. Progress Report
11	11/10 11/12	Current Superscalar Processors Tuesday Classes Meet	Handouts NO CLASS	
12	11/17 11/19	Current Superscalar Processors Multiprocessor/Multi-core	Handouts Ch 4	Midterm exam
13	11/24 11/26	// //	// //	
14	12/1 12/3	//	// //	Prelim. Report
15	12/8 12/10	Project Presentations		Final report