Multiple-Valued Logic Buses for Reducing Bus Size, Transitions and Power in Deep Submicron Technologies

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Abstract

*In this paper, we explore the potential of bus interconnection models using the **Multiple-Valued Logic** paradigm to reduce the power consumption of on-chip address and data buses within embedded SoC platforms. Data is sent over the buses using radix-r number system, i.e. ternary, balanced ternary or quaternary, rather than binary. This allows more compact bus design with less number of bus lines. Reducing the number of bus lines also allows us to increase the distance between the adjacent bus lines using the same silicon area. This further reduces interwire capacitance and may lead to significant on-chip bus power reduction for embedded SoCs designed with deep sub-micron technology. We also analyze the bus switching activity on on-chip address and data buses operating in radix-r number system, and observe that the number of bus transitions in a radix-r bus, particularly in a quaternary bus, is significantly less than the number of bus transitions in a binary bus. Thus, this results in significant power savings in the total on-chip bus power. Our experimental results show that the radix-r bus models replacing 32-bit binary equivalent can provide up to 61% reduction in the address bus power and up to 58% reduction in the data bus power when compared to a binary bus model. Thus, on-chip radix-r bus models can be alternative to the binary one in power-efficient embedded systems.*

1. Introduction

Wires become a real bottleneck as semiconductor technology scales [1]. As more modules are packed into a chip, the complexity of communication between the modules increases. Hence, on-chip communication within a System-on-a-Chip (SoC) becomes crucial in terms of bus power consumption. Bus power consumption depends on several factors such as wire and interwire capacitances (or crosstalk capacitances), switching activity, bus frequency and power supply.

In deep sub-micron technologies, interwire capacitance becomes a more significant factor than wire capacitance in bus power consumption [2] because wire capacitance can be reduced as technology scales. For feature sizes greater than 1μm, the effect of the interwire capacitance is considerably smaller than wire capacitance. However, as the features size goes below sub-micron level, the interwire capacitance can be on several orders of magnitude larger than bus wire capacitance [2]. This becomes very problematic both for bus power consumption and bus delay. The switching activity on the bus is described as the transition between different logic levels and is another major contributor to bus power. On-chip bus power is dominated by switching activity in the individual bus lines as well as the switching activity of the neighboring bus lines.

In this paper, we propose on-chip bus models that carry out data transactions in radix-r number systems, mainly in ternary (radix-3), balanced ternary (radix-3) and quaternary (radix-4). The ternary, balanced ternary and quaternary are the most widely used number systems in Multiple-Valued Logic (MVL). We explore the possibility of using ternary, balanced ternary and quaternary buses for reducing the size, switching activity and power consumption of buses within SoC platforms. Our target system model in **Figure 1** shows a SoC model in which a processor core is connected to other chip modules through on-chip address and data buses, and the SoC communicates with outside through

off-chip buses. We aim at reducing four major components in this paper. **1)** The number of on-chip address and data bus lines, **2)** on-chip interwire capacitance by increasing the wire distance between the bus lines, **3)** on-chip address and data bus switching activity and **4)** on-chip address and data bus power consumption.

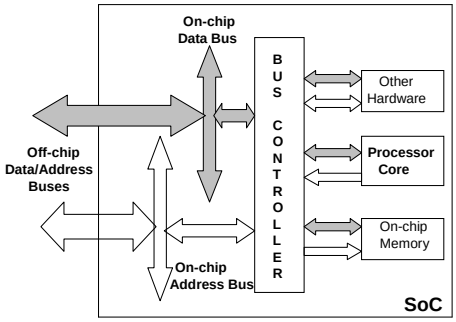

Figure 1 Typical Embedded SoC model and binary buses

The organization of the paper is as follows: *Section 2* talks about the related work. Then, *Section 3* briefly explains the MVL paradigm, its implications on buses and motivates the viability of the use of *radix-r* buses. *Section 4* describes the formulation of the binary and *radix-r* energy consumption models. Next, *Section 5* presents the switching activity of *radix-r* buses and experimental bus energy consumption results using various embedded applications from different benchmark suites. Finally, *Section 6* concludes the paper.

2. Related Work

It is important to note that *radix-r* bus models are not alternative to the techniques proposed to reduce bus switching activity on on-chip *binary* address and data buses such as bus encoding and caching techniques in [19] [20] [21] [22] [23] [24] [25] [26]. These techniques can be orthogonal to a *radix-r* bus, and therefore can be adapted to operate on a *radix-r* bus model to further reduce bus switching activity and bus power.

Bus systems using the multiple-valued logic have been designed by *Beers et al.* [7] that proposes a bi-directional data bus using the MVL paradigm for connecting processors to off-chip caches or memory. *Dhaou et al.* [27] describes a quaternary intermodule communication system using current-mode signaling for DSP processors. They show that the power consumed by the binary-to-quaternary and quaternary-to-binary conversion is negligibly smaller than the power consumed by the interconnection between the modules in deep submicron levels. *Mochizuki et al.* [13] also presents a high-speed on-chip data bus model having the four-valued logic levels using multiple-valued current-mode signaling circuit technique. However, none of these techniques analyze the effects of communicating *radix-r* values over buses for reducing bus switching activity and therefore the total bus energy consumption.

3. Multiple-Valued Logic

MVL circuits have been designed and implemented over last 20 years as an alternative to binary circuits. The advantages of MVL are the use of fewer operations, potentially fewer gates and the reduction in the number of interconnections such as buses where a bus line operating under a *radix-r* number system can contain more information than a binary equivalent.

There have been several attempts [4] [5] [6] [8] [9] to design mixed binary and MVL circuits that require the use of *binary-to-radix-r* encoder and *radix-r-to-binary* decoder circuits. Much of the attention has been focused on ternary and quaternary number systems. Ternary system consists of three digits, namely {0, 1, 2} and quaternary system consists of four digits {0, 1, 2, 3}. In fact, *Hurst* in [29] reports that the most efficient base in computations in terms of cost and complexity is *e* (i.e. 2.7…) and 3 is the nearest integer to *e*. Also, balanced ternary number system {-1, 0, 1} has the property of representing both sign and unsigned numbers. Balanced ternary has one advantage over the ternary system that it does not need a sign *trit*. Negative numbers are naturally represented since the number system has -1 as a digit. A digit is called *trit* and *quatrit* for ternary and quaternary number systems.

Radix-r logic circuits can be implemented using either multiple-valued voltage-mode or current-mode signaling circuit technique. Using voltage-mode signaling, a *radix-r* number system can be represented with multiple voltage levels. However, the disadvantage of defining multiple logic levels using multiple-valued voltage-mode signaling comes with a price of having relatively lower noise margin levels than the binary. On the other hand, current-mode signaling is much faster and more power-efficient than the voltage-mode signaling at deep submicron levels [28]. Unlike multiple-valued voltage-mode, multiple currents determine the logic levels in multiple-valued current-mode signaling. So, it is less susceptible to noise than the voltage-mode signaling.

The *radix-r* and binary logic circuits can also be in the same system where both circuits are interfaced

with each other using conversion circuits. The quaternary number system, in particular, drew special attention because its conversion from/to binary is less complicated than the ternary system. Quaternary logic can be interfaced with binary logic using fast conversion circuits [11] [12].

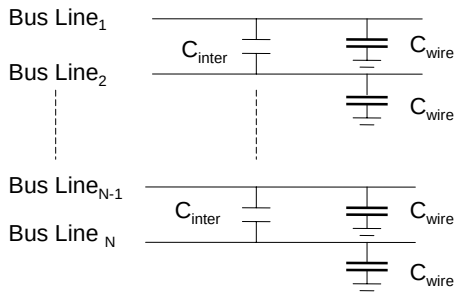

Figure 2 Typical bus model

4. Multiple-Valued Bus Power Modeling

Figure 2 shows an approximate model of a bus. C_{wire} is wire capacitance of each bus line and C_{inter} is interwire capacitance between adjacent bus lines. Interwire capacitance is noise caused by coupling to neighboring wires. It has a very important effect on both power consumption and wire propagation delay as the technology scales. The bus energy consumption is given by the following equation as described by *Sotiriadis et al.* in [3]:

$$E = V_{dd}^2 \left(C_{\text{wire}} \sum_{i=1}^{N} SW_i + C_{\text{inter}} \sum_{j=1}^{N-1} SW_{j,j+1} \right) \quad \textbf{(1)}$$

Energy consumed on each bus line is caused by switching wire and interwire capacitances. Here, V_{dd} is the supply voltage and N is the number of bus lines. SW_i denotes the switching activity of the bus line capacitance i (i.e. *vertical switching activity*), and $SW_{j,j+1}$ represents concurrent switching activity of the neighbor bus line capacitances j and j+1 (i.e. *horizontal switching activity*). A vertical switching activity occurs during consequent data transactions on the bus when the previous value on a bus line changes from 0 to 1 or from 1 to 0. A horizontal switching activity occurs during the same data transaction between the adjacent bus lines. Using *radix-r* logic levels on the buses may have potential positive impact on the switching activity. The total number of vertical and horizontal switching activities on the buses may decrease because the number of bus lines is reduced substantially even though the probability of a transition in an individual bus line and simultaneous transitions in the adjacent lines increases.

We motivate the use of ternary, balanced ternary and quaternary logic for bus communication to reduce on-chip address and data bus sizes, transitions, interwire capacitance and power. The SoC model using *radix-r* on-chip buses is shown in **Figure 3**. The bus controller has built-in *binary-to-radix-r* and *radix-r-to-binary* conversion logic to convert data representation between buses and the SoC units because all the SoC units including the processor and memory operate in binary internally. Several fast and low-power binary-to-radix-r and radix-r-to-binary conversion CMOS logic circuits are already designed as in [10] [11] [12]. We believe that the conversion circuitry can be designed in such a way that it does not add an excessive number of penalty cycles. This argument is supported by the following facts that it takes about 8ns to convert from quaternary to binary in [11]. Similarly, conversion from ternary to binary takes about 9ns according to [12]. Thus, such fast and low-power conversion circuits can be integrated into the existing bus controllers with minimal overhead [13].

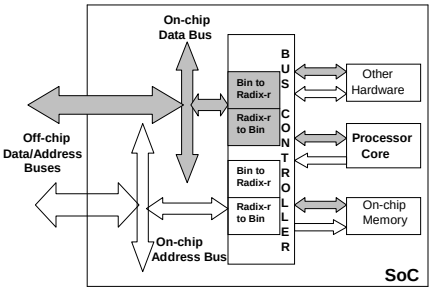

Figure 3 Equivalent SoC model with *radix-r* buses

4.1 Adjustment of Bus Wire Distance

Interwire capacitance gets larger as the distance between adjacent wires gets smaller. Interwire capacitance takes effect during the switching of the line, and this is a bigger contributor to the total bus power than the bus wire capacitance as feature size shrinks. Hence, parallel bus lines should be spaced enough to decrease interwire capacitance but this requires extra silicon area to space the bus lines sufficiently. However, a *radix-r* bus allows us to increase the spacing between the wires using the chip area freed from the eliminated binary bus lines. Not only does this reduce interwire capacitance, but also leads to significant reduction in the total bus power.

Essentially, N-bit bus can be compacted into M lines in *radix-r* number system. The number of *radix-r* bus lines can be found using this equation:

$$M = \frac{N}{\log_2 r} \qquad (2)$$

Reduction in the number of bus lines gives the opportunity of decreasing interwire capacitance between the bus lines. This can be done by increasing the spacing between the wires since capacitance is inversely proportional to the spacing of parallel wires [14]. We can increase the spacing between the *radix-r* bus lines using the silicon area saved by the eliminated binary bus lines. Hence, no extra silicon area needs to be allocated for this purpose. The interwire capacitance of *radix-r* bus can be reduced by a factor that is computed by equally spacing the remaining *radix-r* bus lines. The new spacing between the wires is computed using the following equation assuming the original spacing is 1 unit:

$$rf = 1 + \frac{N - M}{M - 1} = \frac{N - 1}{M - 1} \qquad (3)$$

Here, *rf* represents the reduction factor. The *radix-r* bus interwire capacitance is the binary bus interwire capacitance divided by *rf*. For instance, if the original binary bus size is 8 bits, then the ternary bus size will be 6 *trits*. Now, the new spacing, *rf*, between the ternary bus lines becomes 1.4 units, i.e. each wire is given an equal share (0.4 units) of the remaining silicon area.

Thus, the energy model of a *radix-r* bus can be written as follows:

$$E_r = V_{dd}^2 \left(C_{\text{wire}} \sum_{i=1}^{\frac{N}{\log_2 r}} SW_i + \frac{C_{\text{inter}}}{rf} \sum_{j=1}^{\frac{N}{\log_2 r}-1} SW_{j,j+1} \right) \qquad (4)$$

5. Experimental Results

The hardware design of bus controllers including bus receivers/drivers along with binary-to-radix-r/radix-r-to-binary conversion logic and the analysis of their energy consumption is beyond the scope of this paper. Thus, the main focus of this section is to compare the energy consumption of the binary bus to that of the *radix-r* bus by analyzing the characteristics of data transactions over the buses for several embedded applications.

Thus, we provide empirical results in this section to measure on-chip address and data bus power consumptions. We run several embedded benchmarks from *MediaBench* [17], *MiBench* [18] and *NetBench* [16] as shown in **Table 1**. We use the *SimpleScalar 3.0d* [15] simulator to generate and observe address and data bus transactions, and then estimate the total bus power consumption for binary, ternary, balanced ternary and quaternary bus models by measuring the switching activity of each model. The address and data bus sizes are 32-bits long in binary. This is 21 and 20 trits for the ternary and balanced ternary and 16 quatrits for the quaternary bus models.

Table 1 Benchmarks

MediaBench	*adpcm encoder, unepic, mpeg2decoder, cjpeg, g721encoder, gsm encoder*
MiBench	*sha, fft, rijndael*
NetBench	*crc, route, md5, tl, url, drr, dh*
Other	*fir, sobel* (edge detection), *matmul* (matrix multiplication), *k-means clustering*, *rse* (Reed-Solomon error correction)

For each bus model, we measure the number of vertical and horizontal switching activities on the address and data buses. Then, we present energy consumption results of all bus models for two feature sizes, *3µm* (*i.e. over micron*) and *65nm* (*i.e. deep submicron*) to show the viability of the *radix-r* bus in deep sub-micron technologies. For a given feature size, the wire and interwire capacitances are calculated from *the capacitance-feature size trend graph* provided in [2]. The bus power consumption of each bus model is estimated after computing the number of vertical and horizontal switching activities using **Equation 1** and **4**. For all graphs in this section, the percentage reduction rates are presented with respect to the binary model.

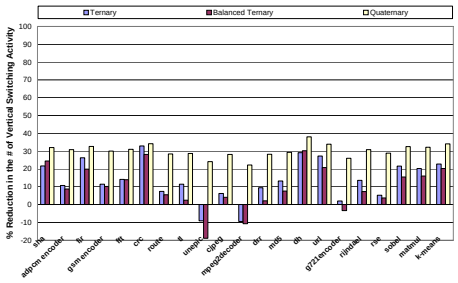

Figure 4 Percentage reduction in the number of the address bus vertical switching activities (negative bars imply the percentage increase in switching activity)

5.1 Address Bus Analysis

Figure 4 and **Figure 5** show the percentage reductions in the number of vertical and horizontal switching activities on the address bus. The quaternary

bus model has a smaller number of switching activities than the binary bus model for all benchmarks. For most of the benchmarks, the ternary and balanced ternary bus models have fewer switching activities than the binary. The ternary model has more vertical switching activities than the binary for *unepic* and *mpeg2decoder*. The balanced ternary model follows the similar pattern for these benchmarks also including *g721encoder*. As for the horizontal switching activity, the ternary model has more activities in *route* and *drr* than the binary. Similarly, *tl* and *drr* are the benchmarks that have more horizontal switching activities in the balanced ternary than the binary. So, the ternary and balanced ternary model may encounter bus power increase rather than power reduction for these benchmarks.

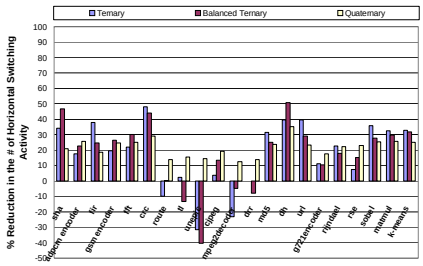

Figure 5 Percentage reduction in the number of the address bus horizontal switching activities (negative bars imply the percentage increase in switching activity)

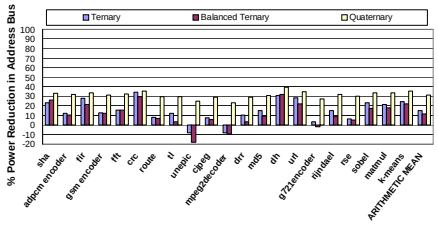

Figure 6 Power results for on-chip address bus using 3µm feature size (negative bars imply the percentage increase in power)

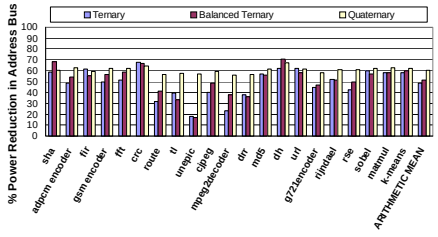

Figure 7 Power results for on-chip address bus using 65nm feature size

Figure 6 and **Figure 7** show the power results for on-chip address bus using 3µm and 65nm feature sizes. The quaternary bus model performs the best out of all bus models. On average, the quaternary, ternary and balanced ternary models have power reduction rates of 31%, 15% and 11%, respectively for 3µm technology. The ternary and balanced ternary models increase power consumption for *unepic* and *mpeg2decoder* due to a large number of horizontal and vertical switching activities. Also, an increase in power consumption is observed in *g721encoder* for the balanced ternary model for the same reason. So, reduction in the interwire capacitance by wire spacing for the ternary and balanced ternary is not sufficient to reduce the total bus power more than the binary bus for 3µm. However, this is sufficient in *route* and *drr* for ternary, and in *tl* and *drr* for balanced ternary. Both bus models have power reductions in these benchmarks even though they have worse switching activities than the binary. As the feature size decreases to 65nm (i.e. deep sub-micron), the interwire capacitance increases significantly for all bus models but the *radix-r* bus models can offset this by wire spacing as seen in **Figure 7**. Now, all bus models have significant power reduction rates for all benchmarks. On average, the quaternary, ternary and balanced ternary models have on-chip address power reduction rates of 61%, 49% and 52%, respectively for 65nm technology.

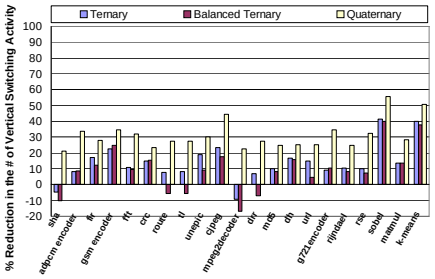

Figure 8 Percentage reduction in the number of the data bus vertical switching activities (negative bars imply the percentage increase in switching activity)

5.2 Data Bus Analysis

Figure 8 and **Figure 9** show the percentage reductions in the number of vertical and horizontal switching activities on the data bus. The amount of vertical switching activity for the quaternary model is better than the binary for all benchmarks. For ternary, only *sha* and *mpeg2decoder* encounter increases in the vertical activity. The same situation is observed in *sha, route, tl, mpeg2decoder* and *drr* for balanced ternary.

The increase in the horizontal switching activity becomes drastic for the ternary and balanced ternary models, particularly in *sha* and *mpeg2decoder*. Even the quaternary model sees a slight increase in the vertical activity in *sha, crc, mpeg2decoder, md5, dh* and *rijndael*.

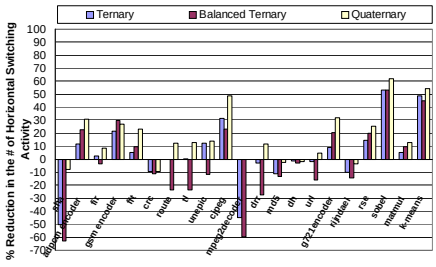

Figure 9 Percentage reduction in the number of the data bus horizontal switching activities (negative bars imply the percentage increase in switching activity)

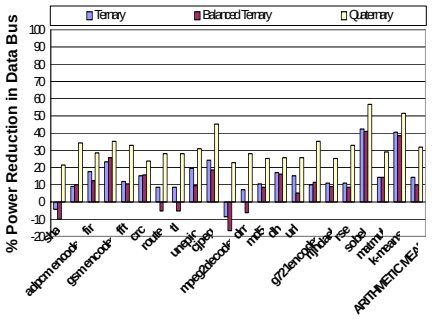

Figure 10 Power results for on-chip data bus using 3µm feature size (negative bars imply the percentage increase in power)

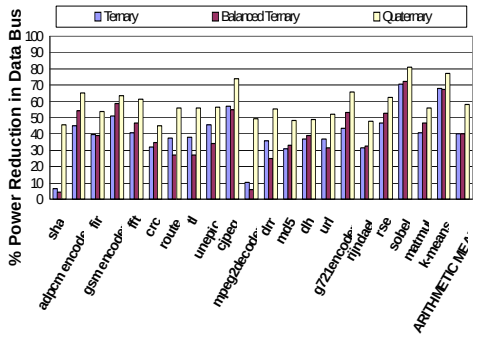

Figure 11 Power results for on-chip data bus using 65nm feature size

Figure 10 and **Figure 11** show the power results for on-chip data bus using 3µm and 65nm feature sizes. Similar to the address bus case, the quaternary bus model outperforms all the bus models. On average, the quaternary, ternary and balanced ternary models have power reduction rates of 31%, 14% and 10%, respectively for 3µm technology. The bus power consumption for the ternary model increases for *sha* and *mpeg2decoder*. The same observation can be made for *sha, route, tl, mpeg2decoder* and *drr* for the balanced ternary model. Particularly, the increase in *sha* and *mpeg2decoder* for balanced ternary is significantly large at about 10% and 17%, respectively. Even though the interwire capacitance of the ternary and balanced ternary bus models is a lot smaller than the binary, it does not suffice to offset the large number of horizontal switching activities on the bus lines. However, the picture changes when the feature size becomes 65nm as shown in **Figure 11**. Now, all three bus models have power reductions for all the benchmarks. We even observe that both the ternary and balanced ternary models reduce the bus power in *sha* and *mpeg2decoder*. Using 65nm technology, an average of 40%, 40% and 58% reduction rates is possible for the ternary, balanced ternary and quaternary bus models, respectively.

In summary, the quaternary bus model is superior to the binary, ternary and balanced ternary bus models in terms of dynamic bus power reduction. Also, it can reduce the bus size by half. In contrast, the ternary and balanced ternary bus models suffer from an increase in the on-chip bus power consumption for high feature sizes. However, as the technology scales down, the dynamic bus power can be reduced significantly using all *radix-r* bus models.

6. Conclusion

We have explored the potential of bus interconnection models using the *Multiple-Valued Logic* paradigm to reduce the size, switching activity, interwire capacitance and power consumption of on-chip address/data buses within embedded SoC platforms. Sending data in *radix-r* number system, instead of binary, allows more compact and power-efficient bus design.

The number of bus lines in a *radix-r* bus is a lot fewer than that of a binary one. We can take advantage of increasing the spacing between the *radix-r* bus lines using the silicon area saved from the eliminated *binary* bus lines. This significantly reduces interwire capacitance, which is a dominating bus capacitance in deep sub-micron technology. We have also shown that the transition activity in the *radix-r* address and data buses is much less than the transition activity in the binary equivalent. Thus, *radix-r* buses may lead to

significant on-chip bus power reduction due to their potential to reduce interwire capacitance and bus switching activity.

We have empirically shown that *radix-r* on-chip buses are viable interconnections inside an embedded SoC for reducing the bus energy as feature size goes down to deep sub-micron levels.

7. References

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