NOTE: The 72 pin module standards that follow describe two separate devices. Both have a 4 byte data interface. One is intended to be used with or without parity bits while the other contains error correction bits ECC). The one with ECC is similar to the parity module but is not completely pin compatible

4.4.2 – 72 PIN SIMM DRAM MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 32 or 36 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES
LOGIC FEATURES, These modules contain a “presence detect” feature which conists of output pins which supply an encoded value which defines the storage capacity and speed of the module.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4.4.2–2A
BLOCK DIAGRAMS—Fig. 4.4.2–2 A–K. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–2 B–K
POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

– 72 PIN SIMM DRAM ECC MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 36 or 39 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES
LOGIC FEATURES, These modules are optimized for ECC applications. They are similar to but not the same as the modules described in Fig. 4–6. The Standard defines a “presence detect” feature which consists of output pins which supply an encoded value which defines the storage capacity and speed of the module. The PD code identifies the presence of an ECC module as well as the speed and organization of the module. The Standard also defines the logic organization of the modules in Figs. 4.4.2–3B & 4.4.2–3C.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4.4.2–3A
BLOCK DIAGRAMS—Figs. 4.4.2–3 B & C. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–3 B & C
POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

72 Pin SIMM Block Diagrams

The block diagrams given in the 12 pages, Figs 4.4.2–2 B ⇒ K and Figs 4.4.2–3 B & C), are applicable to the 72 Pin SIMM pinouts shown in Figures 4.4.2–2 A and 4.4.2–3 A. These block diagrams are provided for guidance only. **Other implementations with different block configurations are also acceptable**.

The following table shows the applicability of the block configurations given to the 5 V and 3.3 V Non–ECC and ECC modules.

Configuration	# Banks	Applies to: 5 V SIMM	Applies to: 3.3 V SIMM
Parity, Non–Parity			
X32/36 W/X4, X1 (X36)	1 or 2	X	X
X32/36 W/X16, X18	1 or 2	X	X
X36 W/X4, X4/4CE	1 or 2	X	X
X36 W/X4, X2/2CE	1 or 2	X	X
X36 W/X16, X4/4CE	1 or 2	X	X
X36 W/X16, X2/2CE	1 or 2	X	X
X32 W/X8	1 or 2		X
X36 W/X8, X2/2CE	1 or 2		X
X32 W/X32	1 or 2		X
X36 W/X32, X2/2CE	1 or 2		X
ECC			
X36/40 W/X4	1 or 2	X	X (X36 only)

Note: To reduce the number of diagrams, only 2 bank versions are shown. In addition, in cases where one SIMM I/O width can be described as a depopulation of another SIMM (i.e. X36⇒X32), the depopulated devices are shown by a "dashed" outline.

$\overline{RE}$ AND $\overline{G}$ WIRING FOR BYTE WRITE SIMMS.		
SIGNAL NAME	5 V SIMMs	3.3 V SIMMs
$\overline{G}$	Tied to GND	Wired to Pin 46
$\overline{RE0}$	Connected as shown. Tied to pin 44 ($\overline{RE0}$)	$\overline{RE0}$, $\overline{RE2}$ nets connected together and tied to pin 44 ($\overline{RE0}$)
$\overline{RE1}$	Connected as shown. Tied to pin 45 ($\overline{RE1}$)	$\overline{RE1}$, $\overline{RE3}$ nets connected together and tied to pin 45 ($\overline{RE1}$)
$\overline{RE2}$	Connected as shown. Tied to pin 34 ($\overline{RE2}$)	$\overline{RE0}$, $\overline{RE2}$ nets connected together and tied to pin 44 ($\overline{RE0}$)
$\overline{RE3}$	Connected as shown. Tied to pin 33 ($\overline{RE3}$)	$\overline{RE1}$, $\overline{RE3}$ nets connected together and tied to pin 45 ($\overline{RE1}$)

FIGURE 4.4.2–1
72 PIN DRAM SIMM APPLICABILITY TABLE

	5 V Byte Write	3.3 V Byte Write		5 V Byte Write	3.3 V Byte Write
PIN #	PIN NAME	PIN NAME	PIN #	PIN NAME	PIN NAME
1	VSS	VSS	37	PDQ17, NC	PDQ17, NC
2	DQ0	DQ0	38	PDQ35,, NC	PDQ35,, NC
3	DQ18	DQ18	39	VSS	VSS
4	DQ1	DQ1	40	$\overline{CE0}$	$\overline{CE0}$
5	DQ19	DQ19	41	$\overline{CE2}$	$\overline{CE2}$
6	DQ2	DQ2	42	$\overline{CE3}$	$\overline{CE3}$
7	DQ20	DQ20	43	$\overline{CE1}$	$\overline{CE1}$
8	DQ3	DQ3	44	$\overline{RE0}$	$\overline{RE0}$
9	DQ21	DQ21	45	NC, $\overline{RE1}$	NC, $\overline{RE1}$
10	VDD	VDD	46	NC	$\overline{G}$
11	NU	PD5	47	$\overline{W}$	$\overline{W}$
12	A0	A0	48	PD(ECC)	PD(ECC)
13	A1	A1	49	DQ9	DQ9
14	A2	A2	50	DQ27	DQ27
15	A3	A3	51	DQ10	DQ10
16	A4	A4	52	DQ28	DQ28
17	A5	A5	53	DQ11	DQ11
18	A6	A6	54	DQ29	DQ29
19	NC, A10	NC, A10	55	DQ12	DQ12
20	DQ4	DQ4	56	DQ30	DQ30
21	DQ22	DQ22	57	DQ13	DQ13
22	DQ5	DQ5	58	DQ31	DQ31
23	DQ23	DQ23	59	VDD	VDD
24	DQ6	DQ6	60	DQ32	DQ32
25	DQ24	DQ24	61	DQ14	DQ14
26	DQ7	DQ7	62	DQ33	DQ33
27	DQ25	DQ25	63	DQ15	DQ15
28	A7	A7	64	DQ34	DQ34
29	NC, A11	NC, A11	65	DQ16	DQ16
30	VDD	VDD	66	NC	$\overline{EDO}$
31	A8	A8	67	PD1	PD1
32	NC, A9	NC, A9	68	PD2	PD2
33	NC, RE3	NC, A12	69	PD3	PD3
34	$\overline{RE2}$	NC, A13	70	PD4	PD4
35	PDQ26, NC	PDQ26, NC	71	NC	PD(REF)
36	PDQ8, NC	PDQ8, NC	72	VSS	VSS

See Figure 4–18 for applicable block diagrams

PRESENCE DETECT TRUTH TABLE

CONFIGURATION	tRAC	$\overline{ECC}$	PD1	PD2	PD3	PD4
1MB (256K X 36)	100 nS	O	S	O	S	S
64MB (16M X 32/36)	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
2MB (512K X 36)	100 nS	O	O	S	S	S
128MB (32M X 32/36)	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O
4MB (1M X 36)	100 nS	O	S	S	S	S
256MB (64M X 32/36)	80 nS	O	S	S	O	S
	70 nS	O	S	S	S	O
	60 nS	O	S	S	O	O
8MB (2M X 36)	100 nS	O	O	O	S	S
0.5GB (128M X 32/36)	80 nS	O	O	O	O	S
	70 nS	O	O	O	S	O
	60 nS	O	O	O	O	O
16MB (4M X 36)	50 nS	O	S	O	S	S
1GB (256M X 32/36)	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
32MB (8M X 36)	50 nS	O	O	S	S	S
2GB (512M X 36)	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O

O = NO CONNECTION S = CONNECTED TO VSS

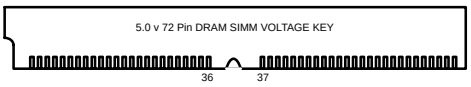
$\overline{EDO}$ Pin: VSS for EDO, NC for Fast Page.

Note: The $\overline{ECC}$ Function (Pin 48) is not a defined function for the devices in this standard, however, it is used in a companion Standard for 72 pin ECC modules shown in Fig. 4.4.2–3. The presence of a VSS connection on this pin signifies that an ECC module has been inserted.

CONFIGURATION PIN ASSIGNMENT TABLE

	MODULE SIZE, 36 BIT WORDS											
PIN #	256K	512K	1M	2M	4M	8M	16M	32M	64M	128M	256M	512M
19	NC	NC	NC	NC	A10	A10	A10	A10	A10	A10	A10	A10
*29	NC	NC	NC	NC	A11	A11	A11	A11	A11	A11	A11	A11
32	NC	NC	A9	A9	A9	A9	A9	A9	A9	A9	A9	A9
*33	NC	$\overline{RE3}$	NC	$\overline{RE3}$	NC	$\overline{RE3}$	A12	A12	A12	A12	A12	A12
*34	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	NC	A13	A13	A13	A13
45	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	RE1

* A11, A12, or A13 on Pins 29, 33, or 34 are used on modules containing devices that require asymetric ROW/ COLUMN addresses.
NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.



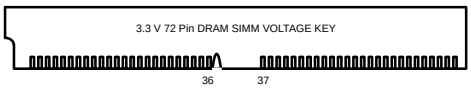


FIGURE 4.4.2–2 A
256K TO 256M BY 36, 72 PIN DRAM MODULE PINOUT

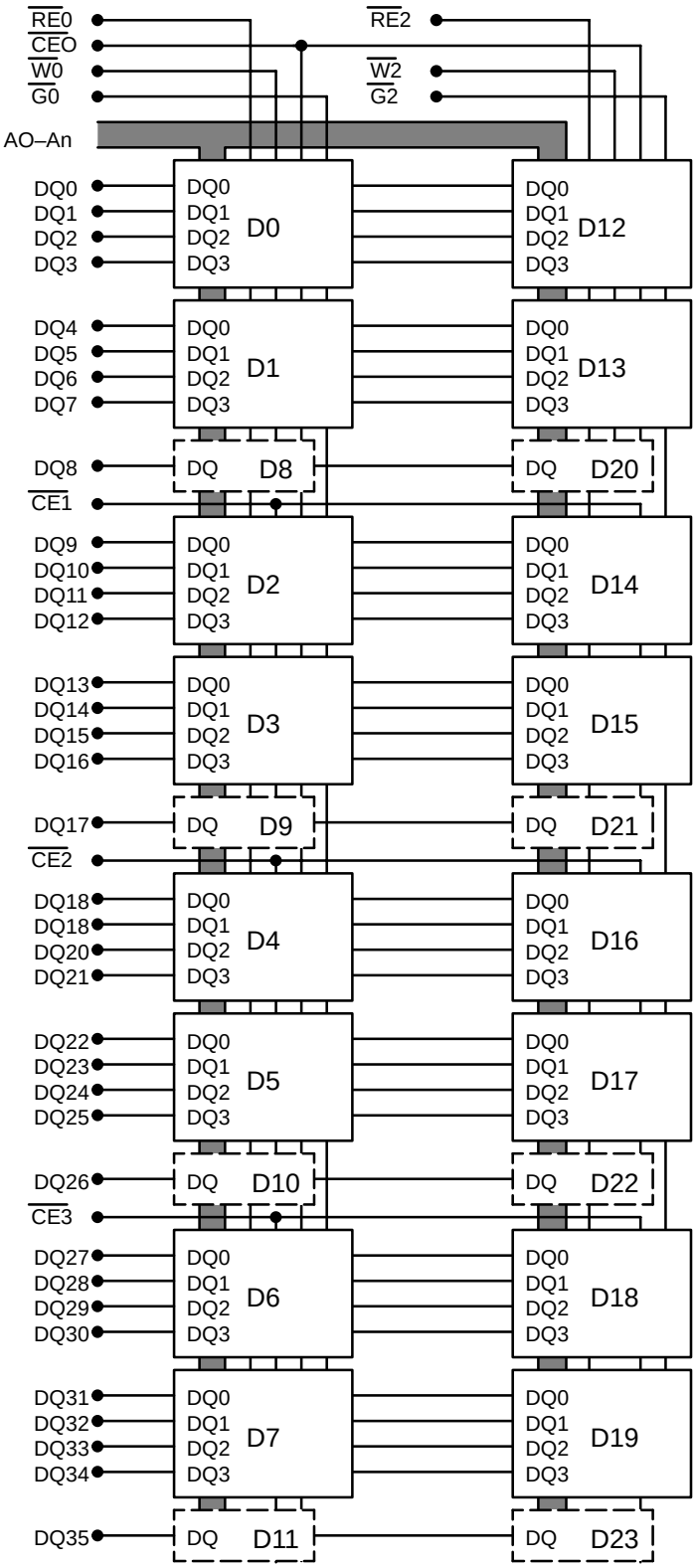


FIGURE 4.4.2–2 B
X32/36 DRAM SIMM, 2 Banks with X4 & X1 DRAMs