Special Session on Design Methods, Tools and Examples for FPGA-Based Acceleration of Artificial Neural Networks at the **IEEE Symposium on Neuromorphic Cognitive Computing**
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SESSION CHAIRS

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OVERVIEW

Reconfigurable architectures are a promising class of computing systems to address many of the performance, scalability, and energy efficiency challenges in neuromorphic computing, in general, and artificial neural network (ANN) based algorithms and applications, in particular. Spatial distribution of the field-programmable gate array (FPGA) logic coupled with its configurability into processing or storage elements lends itself well to the computational characteristics, e.g., processing in memory (PIM), of neuromorphic architectures, or the high degree of communication and processing concurrencies requirements of the NN-based algorithms and applications. The SNCC 2017 special session on "Design Methods, Tools and Examples for FPGA-Based Acceleration of Artificial Neural Networks" aims to spotlight the latest FPGA-based design methodologies, techniques and tools and their applications to the field of artificial neural network algorithms and applications acceleration.

TOPICS

The goal of the special session is to provide a platform for researchers and practitioners from academia, government and industry to present their research results in the area of FPGA-based acceleration of artificial neural network algorithms and applications. Topics of interest include but are not limited to:

- High-level abstractions for designing, optimizing, mapping, partitioning, routing, testing and verifying FPGA domain specific NNs;
- Computer-aided design tools to facilitate the design, development, and deployment of scalable and high-performance FPGA-based NN executions;
- FPGA-aware neural network algorithms development, including network compression methods and weight quantization approaches;
- Novel, high-performance implementations of machine and deep learning algorithms;
- Open-source synthesizable register-transfer level (RTL) platforms enabling faster design and deployment of FPGA-based NN accelerators;
- FPGA-based NN application design studies.

SUBMISSION

Submissions should present novel FPGA-based algorithms, tools, architectures, design, or techniques for the efficient processing of neural network algorithms and applications. More information on paper submission can be found at the SNCC 2017 website at http://www.ele.uri.edu/ieee-ssci2017/SNCC.htm. Please select the category of special session "Design Methods, Tools and Examples for FPGA-Based Acceleration of Artificial Neural Networks" during the paper submission process. All submitted papers will be fully refereed. Accepted papers will be published in the SNCC 2017 Proceedings. All special session submissions are to follow the conference format: 8 pages two-column format.