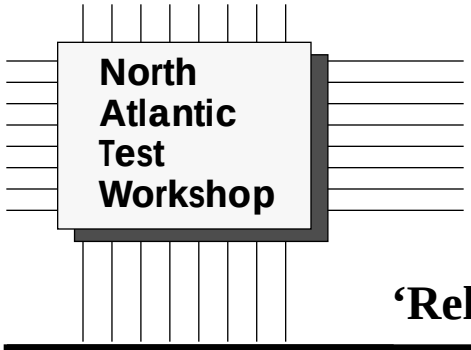

7th IEEE North Atlantic Test Workshop

URI W. Alton Jones Campus
West Greenwich, RI, USA
May 28 - May 29, 1998

'Reliability and Testing Issues for the 21st Century'

Advance Program

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to higher quality, more economical, and more efficient testing methodologies and designs. The 7th workshop will focus on '**Reliability and Testing Issues for the 21st Century**'.

This year's workshop will open with a **keynote talk by Dhiraj K. Pradhan**, COE Endowed Chair at Texas A&M University and IEEE fellow. Dhiraj's talk will focus on the major advances that have been achieved this decade in the area of logic verification and equivalence checking within an ATPG framework. Immediately following will be an **invited talk on 'New Techniques in Testing and Diagnosis for Computer Hardware' by Mark Karpovsky from Boston University**. Mark is the Director of The Reliable Computer Laboratory and a professor at Boston University. He is also an IEEE fellow. The remaining one and one-half days of technical papers will include many other interesting topics, presented by researchers and practitioners in the field.

The 1998 workshop will be held at the Whispering Pines Conference Center, located on the W. Alton Jones Campus of the University of Rhode Island. URI's W. Alton Jones Campus is situated on 2,300 acres of pristine forest, streams, ponds, a 75 acre lake, and a nineteenth-century farm. The campus adjoins the 40,000 acre Arcadia and Pachaug State Forests. It is a 30 minute drive from Providence, RI, a 1 hour and 30 minute drive from Boston, MA or Hartford, CT, and a 3 hour drive from New York City.

For information contact:

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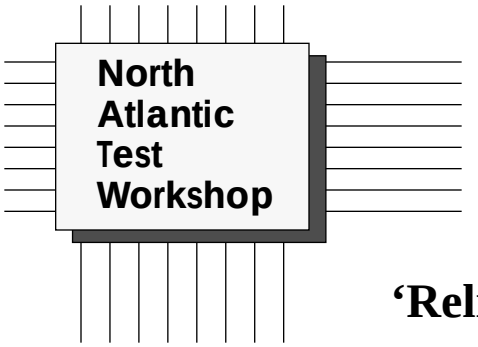
To view other information regarding this workshop, visit our home page. The URL is **http://www.ele.uri.edu/natw98**

The 1998 North Atlantic Test Workshop is sponsored by the **University of Rhode Island** and the **IEEE Computer Society Test Technology Technical Committee.**



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Workshop Registration

All workshop functions will be held at the Whispering Pines Conference Center. The workshop registration fee includes breakfast and break refreshments on Thursday and Friday, lunch and dinner on Thursday, and a copy of the digest of papers.

	Advance Registration (postmarked by May 6)	At Door Registration (after May 6)
IEEE member	$210	$260
Non member	$270	$320
Students	$130	$150

Special Meal Requests: (e.g. vegetarian) _____

IEEE No._____

Make check payable to: IEEE, NATW

(Only checks in US Dollars drawn on a US Bank will be accepted)

Name:_____ Company:_____

Address: _____ Telephone:_____

City:_____State:_____ Fax: _____

Zip Code:_____ Country:_____

E-mail: _____

Send full payment with a copy of this form to:

Prof. E. S. Cooley
Thayer School of Engineering
8000 Cummings Hall
Dartmouth College
Hanover, NH 03755-8000

Phone: 603-646-2807
Fax: 603-646-3856
Email: edmond.cooley@dartmouth.edu

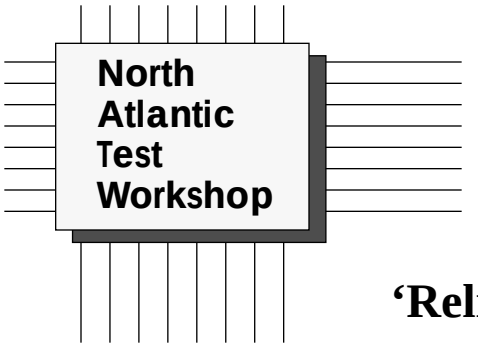
Hotel Registration

Hotel reservations are the responsibility of the attendee.

The cut-off date for guaranteed reservations at the following rate is 5/6/98.

Whispering Pines Conference Center
URI W. Alton Jones Campus
401 Victory Highway
West Greenwich, RI 02817

Phone: 401-397-3361
Fax: 401-397-6540
$107 per night
$28 for Wednesday (5/27) dinner (optional).



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'Reliability and Testing Issues for the 21st Century'

Advance Program

Thursday, May 28, 1998

[8:00 am - 9:00 am] **Registration, Breakfast**

[9:00 am - 10:30 am] **Opening Session**

Welcome: *Jim Monzel,* IBM; *Karen Lentz*, Tufts University

Keynote Speech: 'Recent Advances in ATPG Based Verification',
Dhiraj Pradhan, Texas A&M University

Invited Talk: 'New Techniques in Testing and Diagnosis for Computer Hardware: Developments from The Reliable Computer Laboratory at Boston University',
Mark Karpovsky, Boston University

[10:30 am - 11:00 am] **Break**

[11:00 am - 12:30 am] **Session 1: Advanced Fault Modeling and Simulation**

Chair: *X. Chen,* IBM

1.1 **'Fault Modeling Analysis Methodology Illustrated with a Dynamic Logic Circuit'**,
R.D. Adams, E.S. Cooley,* Dartmouth College

1.2 **'Concurrent Behavioral Fault Simulation'**,
J. Heller, K. Lentz,* Tufts University

1.3 '**Feasibility of a Redundancy Free Concurrent Error Detection Method'**,
J.C. Lo, University of Rhode Island

[12:30 am - 1:30 pm] **Lunch**

[1:30 pm - 3:30 pm] **Session 2: Automatic Test Pattern Generation**

Chair: *Z. Navabi,* Northeastern University

2.1 **'ATPG based on Genetic Manipulation Techniques'**
H.-CH. Dahmen, U. Glaeser,* GMD-SET

2.2 **'Hierarchical Test Generation with Multi-Level Decision Diagram Models'**,
G. Jervan, A. Markus, J. Raik, R. Ubar,* Tallinn Technical University

2.3 **'A Highly Efficient Weight Generation Method For Handling Very Large Fan in and XOR Tree Designs'** *P. Chang*, B. Keller, T. Snethen,* IBM

2.4 **'A Testability Measure as a Test Pattern Generation Cost Function',**
S. Frenkel, Russian Academy of Sciences

[3:30 pm - 4:00 pm] **Break**

[3:30 pm - 5:30 pm] **Session 3: Testing Systems on a Chip**

Chair: *R. Davies,* DEC

3.1 '**Techniques for Standardizing Analog Core Test Interfaces'**,
D. Firth, B. Cummings,* IBM

3.2 **'Fault Detection using EMR Signature Analysis in ICs and Core-Based Architectures',** *S. Athan,* University of South Florida

3.3 **'Design for Test Challenges and Strategies for System On a Chip Designs',**
F. Meyer, Qualis Design Inc., *J. Monzel*,* IBM

[5:30 pm - 6:00 pm] **Open**

[6:00 pm - 9:00 pm] **Reception / Dinner**

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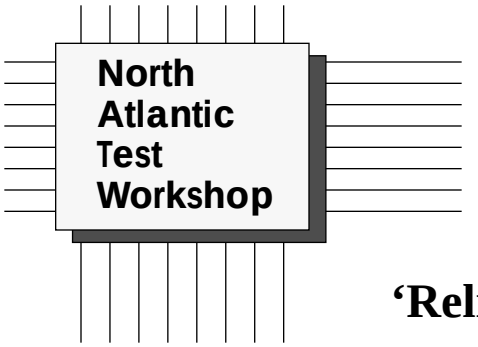

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'Reliability and Testing Issues for the 21st Century'

Advance Program (Continued)

Friday, May 29, 1998

[8:30 am - 9:00 am] **Registration, Breakfast**

[9:00 am - 10:30 am] **Session 4: Clocking and Delay Testing**
Chair: *E. S. Cooley,* Dartmouth

4.1 **'Diagnosing AC Defects of a IBM S/390 Microprocessor',**
P. Song, R. Clairmont, R. Rizzolo, J. L. Lee*, IBM

4.2 **'Clock Template Evaluation: An Industrial Case Study',**
J. Watkins, X. Chen, C. Asher, N. Bourbakis*, IBM

4.3 **'Practical Considerations for Improving Delay Fault Tests Using a Unified Delay Fault Model'**, *R. Jayabharathi*, Intel, *H. Chang*, Soongsil University, *J. Abraham**, University of Texas at Austin

[10:30 am - 11:00 am] **Break**

[11:00 am - 12:30 pm] **Session 5: Synthesis and Testing of Structured Systems**
Chair: *J. Karrfalt,* ASC Inc**.**

5.1 **'Experimentation of Structured Systems'**,
C. Baron, J.C. Geffroy, M. Etchenberia*, INSA-DGEL, LESIA

5.2 **'A Test Synthesis Methodology Using Shared I/O Building Blocks'**,
*L. Smudde**, IBM, *D. Kucharski*, Rochester Institute of Technology,
V. Chickermane, S. Richter, IBM

5.3 **'Testing ROMs Embedded in Deep Submicron ASIC Chips'**
L. R. Brooks, R. L. Barry, J. A. Monzel,* IBM

Close

* Presenter
Note: Each presentation will consist of 20-25 minutes of presentation followed by 5-10 minutes Q&A.