Mixed Signal Testing: Trends and Challenges

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IEEE North Atlantic Test Workshop
May 27 & 28, 1999

Opening Question:

- **Why would a person who has been working on digital systems for 30 years now want to talk about analog and mixed signal systems?**

–or

- Why I moved from **Digital** Equipment to **Analog** Devices when the world is clearly going digital….

The Internet changes everything

- **Major shifts(advances) is computing**
  - > **Standalone Computing**
    - ▫ **1949**
  - > **Batch processing**
    - ▫ **1955/60**
  - > **Timesharing**
    - ▫ **1965/70.**
  - > **Personal Computing (PC's and Workstations)**
    - ▫ **1981**
  - > **Internet**
    - ▫ **1994**
- ***What's Next?***

Ubiquitous Computing

- **The Internet disappears into the fabric of everyday life.**

- **Why would you want this to happen?**
  - **>Examples from Things That Think Program**
  - **>Examples from Xerox Parc U.C. Program**
- **Why will this be possible?**
  - **>IPv6. Next version of Internet protocol**
  - **>Single chip web servers**

- *Hence need for integrated sensor/digital systems.*
  - *>Example: ADuC816*

General Trends

- **Semiconductor speeds are increasing at 30% to 40% per year.**

- **Test system speeds are increasing at 12% per year (at best)**

- **Yield versus Test Accuracy**

Year of First Product Shipment	**1997**	**1999**	**2002**	**2005**	**2008**	**2011**
Yield (%)	90	87	79	75	64	52
Device Period (ns)	1.3	1.1	0.77	0.59	0.43	0.33
Test Accuracy (ns)	0.2	0.2	0.18	0.175	0.175	0.175

The International Technology Roadmap For Semiconductors: 1998 Update

- **High end test has cost around $10K per pin for the last 20 years**
- **Advances in CMOS technology are only part of the solution/(problem)**
  - > **+ cost of memory**
  - > **+ logic for complex microcodes**
  - > **- clock distribution**
  - > **- critical timing components**
  - > **- pin electronics**
- **A breakthrough in technology is needed. SiGe?**

Mixed Signal Test Equipment Requirements

From The National Technology Roadmap For Semiconductors: Technology Needs

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2002* *130 nm*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*
Low Frequency Source & Digitizer						
BW (MHz)	2	15	100	100	100	100
Fs MS/s	5	5	5	10	10	10
Bits	20-23	20-23	20-23	20-23	20-23	20-23
Noise floor (dB/RT Hz)	-130	-155	-160	-160	-160	-160
High Frequency Waveform Source						
Level V (pk-pk)	4	4	4	4	4	4
BW (MHz)	500	800	2000	2500	3000	3000
Fs (MS/s)	1000	2000	5000	6000	7500	7500
Bits AWG/Sine	10/14	10/14	10/14	10/14	10/14	10/14
Noise floor (dB/RT Hz)	-80	-86	-100	-100	-100	-100
High Frequency Waveform Digitizer						
Level V (pk-pk)	4	4	4	4	4	4
BW (MHz) (undersampled)	750	1000	1500	2000	3000	3000
Fs (MS/s)	1/40	1/40/80	1/40/160	1/40/320	1/40/640	1/40/1280
Bits	16/12	16/12/10	16/12/10	18/14/12	18/14/12	20/16/12
Noise floor (dB/RT Hz)	-80	-86	-100	-120	-120	-120
High Speed Sampler						
BW (GHz)	1	2.3	5	5	5	5
Resolution (bits)	16	16	16	16	16	16

Mixed Signal Test Equipment Requirements (Cont.)

From The National Technology Roadmap For Semiconductors: Technology Needs

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2002* *130 nm*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*
Time Measurement						
Jitter measurement (ps RMS)	30	4	4	2	2	2
Frequency measurement (MHz)	250	500	1000	2000	3000	3000
Single shot time capability (ps)	100	100	50	30	30	30
RF/Microwave Instrumentation						
Source BW (GHz)	6	10	18	24	30	36
Source phase noise low frequency (dBc/Hz)	126	130	136	136	136	136
Source phase noise high frequency (dBc/Hz)	150	155	160	160	160	160
Receive BW (GHz)	6	10	18	24	30	36
Receive noise floor (dBm/Hz)	-150	-155	-160	-160	-160	-160
Receive dynamic range SFDR (dB)	60	70	80	80	90	90
Special Digital Capabilities						
D/A and A/D source/capture rate (Mbits/s)	100	200	400	400	500	600
Serial data rate (Mbits/s)	2000	3000	4000	4000	4000	4000

Example: the AD977. A 16bit 100Ksps ADC.

- **The AD977 and AD977A are high speed, low power 16-bit A/D converters, each operating from a single 5 V supply.**
- **The AD977A has a throughput rate of 200 ksps whereas the AD977 has a throughput rate of 100 ksps.**
- **Each part contains a successive approximation, switched capacitor ADC, an internal 2.5 V reference, and a high-speed serial interface.**
- **The ADC is factory calibrated to minimize all linearity errors. The AD977 and AD977A are specified for full-scale bipolar input ranges of ±10 V, ±5 V and ±3.3 V, and unipolar ranges of 0 V to 10 V, 0 V to 5 V and 0 V to 4 V.**
- **The AD977 and AD977A are comprehensively tested for ac parameters such as SNR and THD, as well as the more traditional dc parameters of offset, gain and linearity.**
- **The AD977 and AD977A are available in skinny 20-pin DIP, 20-pin SOIC, and 28-pin SSOP packages.**
- **Typical ASP(I.e. 'street price'): $5.00.**

Testing Time

- **Dominated by Linearity Test.**

- **Need 64 samples per code**
- **2**16 codes, or about 64K codes.**
- **Total of 4M samples needed.**

- **AD977 runs at 100Ksps**
- **Therefore: 40sec of test time for linearity test**

- **Total Test time 45 sec.**

- **If customer wants testing at temperature limits--multiple 45 secs by number of temperatures tested.**

Cost of Test

- Tester: $1M Teradyne
- Assumptions
  - > 5 year life
    - Reality is a range of 3 to 8 year life.
  - > Run 4 40hour shifts/week
    - 160 hours/weeks is pushing the limit
  - > Run 50 weeks/year
    - At least two weeks/year needed for maintenance
  - > Tester running at 50% duty cycle.
    - Time needed to change package handling
    - Time needed to change software for different parts
- Conclusion
  - > 72M seconds of active test time in life of tester.
  - > 1.39 cents/sec of mfg. test
  - > AD977 with 45 sec of test: $0.625 cost of test.
  - > Assuming 50% margin, test 25% of total cost.

Factors Impacting Cost

- **Factors that will increase cost above $.625 or 16bit ADC**
  - > **Multiple temperature testing**
  - > **Utilization of tester**
    - ▫ **Less than 4 shifts/week**
      - – 3 shifts not atypical
    - ▫ **Less than 50 weeks/year**
      - – 50 weeks is typical
    - ▫ **Less than 50% active in test**
      - – 20% or even 10% active time experienced!
    - ▫ **Less than 5 year life.**
      - – 5 years is fairly typical.
  - > **Price of Test Equipment.**
    - – $2M or even $6M not uncommon.
  - > ***Given above: test time can easily go 4X to $2.50 per part! Driving margin to zero.***

Package Types Compounding Cost Problem

- **Qualified Packages at ADI:**
  - > **1996: 90**
  - > **1999: 160**
- **CSP/Chip Scale Packaging**
  - > **Strong customer requirements for CSP**
  - > **CSP will proliferate even more packages**
    - **Less than 20% more area than chip implies large choice in X and Y dimensions to match chip sizes.**
    - **Small physical dimensions makes contacting and handling more difficult**

Factors Impacting Cost (continued)

- ***Factors that could decrease cost below $.625***

- **Increase hours/week from 160 to 168 (very unlikely)**
- **Increase weeks/year from 50 to 52 (very unlikely)**
- **Increase active test time**
  - > **Possible on highest volume parts**
    - **16 bit, 100Ksps ADC unlikely**
  - > **Possible with more flexible package handlers**
    - **However, CSP making this more difficult.**
- **Lower cost of Tester.**
  - > **ADI mfg. some testers internally to reduce cost**
    - **make aggressive use of std. Computers, VME modules, PC's for control, etc.**
- **Reduce the number of tests/code element**
  - > **Research needed in ADC architectures**
  - > **Advanced use of Statistics/design of experiments.**

Summary

- **The Internet is changing everything**
  - **>Mixed signal SOC's only way to interface to the real world.**
- **Testing, especially analog testing, is in danger of dominating mfg. costs.**
- **Interesting research areas in BIST/DFT and better algorithms for testing analog blocks in mixed signal chips.**