AMP1C_50 Amplifier

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Two−Stage CMOS Amplifier

(Amp1n_50)

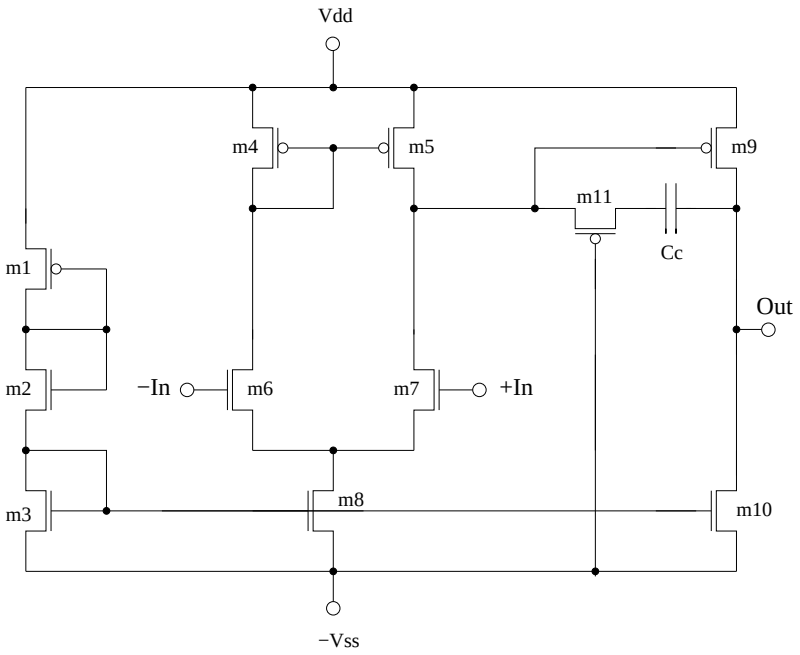

Figure 1: Schematic of the AMP1C_50

Parameter	Simulated Value
Voltage Swing	$\pm$ 1.4V
Open Loop Gain	86dB
Gain Bandwidth	1.1MHz
Phase Margin	71^o
Slew Rate @ C_l=.5pF	$0.30\frac{V}{\mu s}$
CMRR @ DC	126dB
CMRR @ AC 100KHz	92dB
PSRR+ @ DC	92dB
PSRR+ @ AC 100KHz	20dB
PSRR- @ DC	91dB
PSRR- @ AC 100KHz	61dB
Power Supply Rails	$\pm$ 1.5V
$I_{V_{ss}}$	.98μA

Table 1: **Various Parameters of the AMP1C_50 from Simulation**

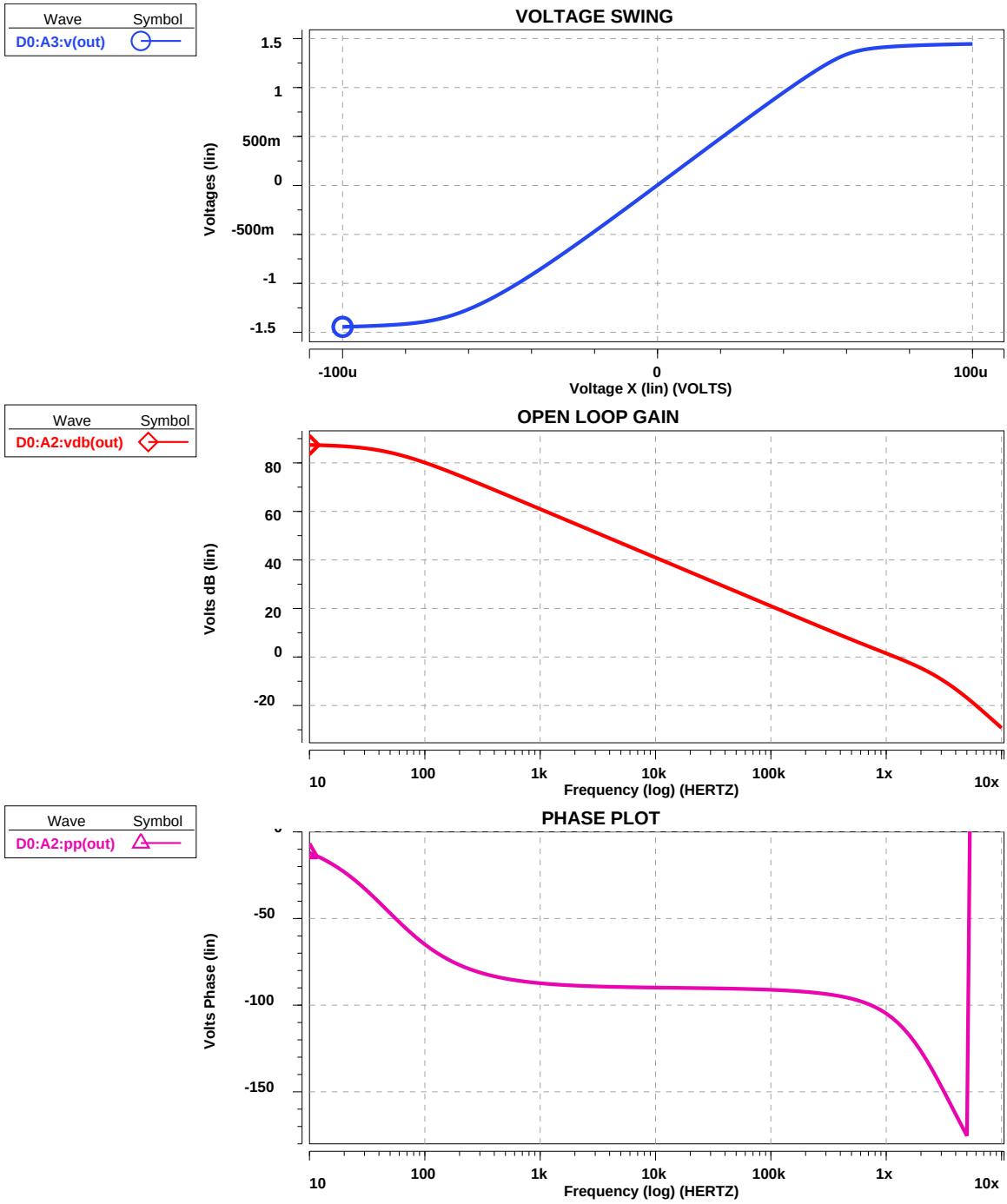

Figure 2: AMP1C_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

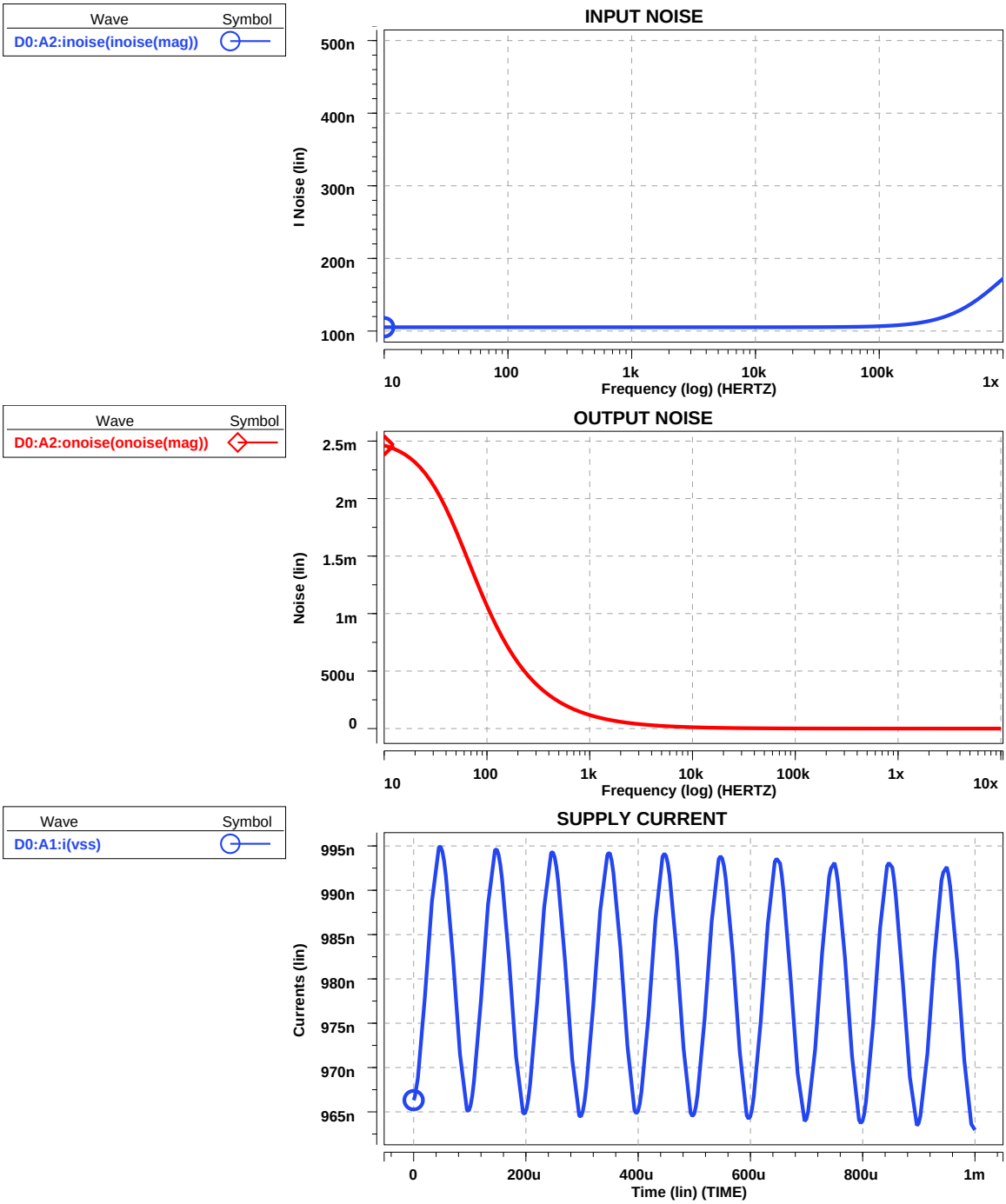

Figure 3: AMP1C_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

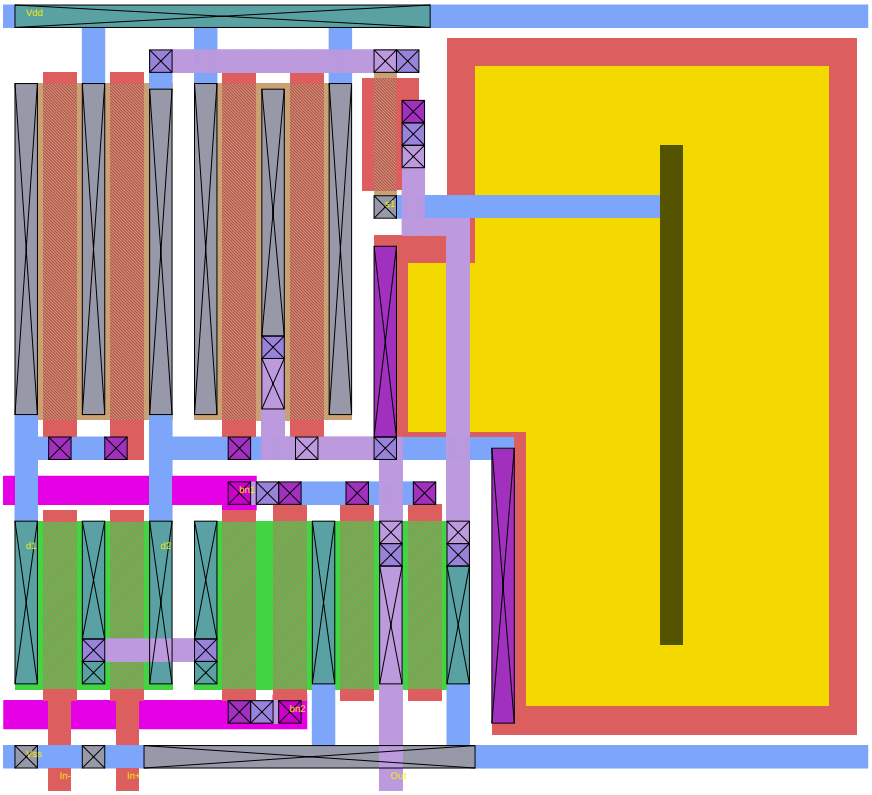

Figure 4: AMP1C_50 Magic Layout 0.5μm Process