# AMP1D_50 Amplifier

Dr. Godi Fischer
Department of Electrical Engineering
University of Rhode Island
fischer@ele.uri.edu

April 18, 2002

Two−Stage CMOS Amplifier
(Amplifier Amp1d_50)

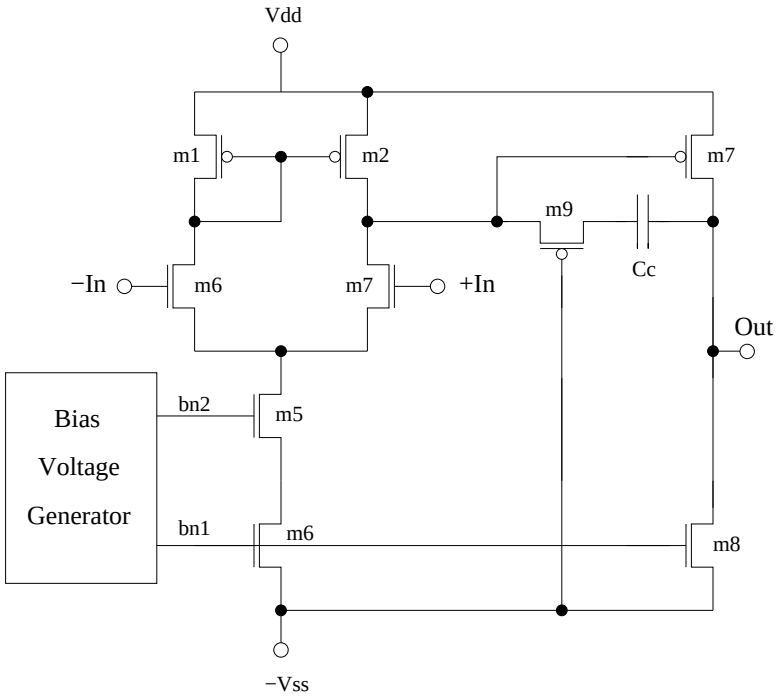


Figure 1: Schematic of the AMP1D_50

| Parameter | Simulated Value |
|---|---|
| Voltage Swing | $\pm$ 1.4V |
| Open Loop Gain | 85dB |
| Gain Bandwidth | 560KHz |
| Phase Margin | $81.9^o$ |
| Slew Rate @ $C_l$=.5pF | $.16\frac{V}{\mu s}$ |
| CMRR @ DC | 130dB |
| CMRR @ AC 100KHz | 75dB |
| PSRR+ @ DC | 89dB |
| PSRR+ @ AC 100KHz | 22dB |
| PSRR- @ DC | 89dB |
| PSRR- @ AC 100KHz | 22dB |
| Power Supply Rails | $\pm$ 1.5V |
| $I_{V_{ss}}$ | $.682\mu$A |

Table 1: **Various Parameters of the AMP1D_50 from Simulation**

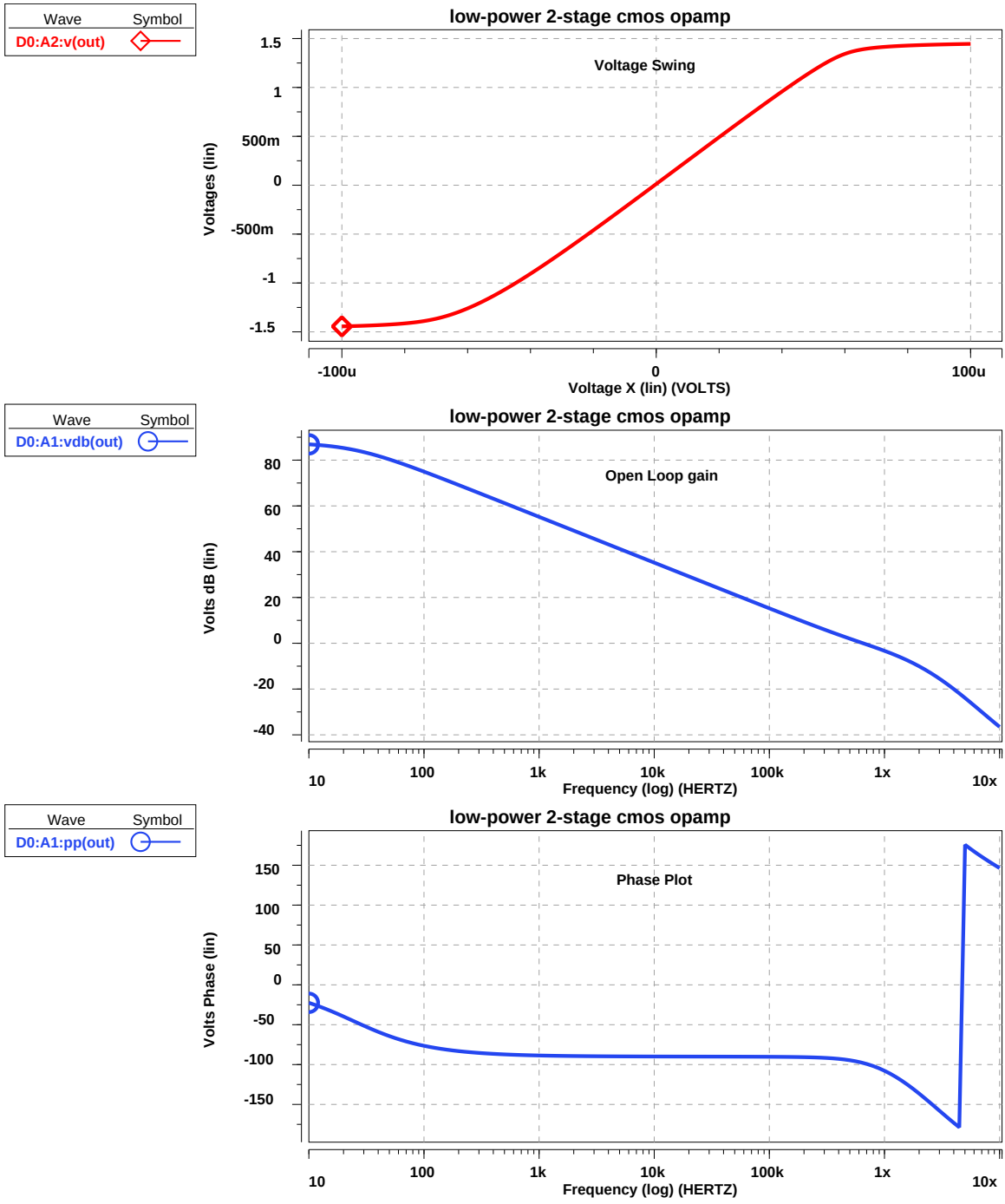


Figure 2: AMP1D_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

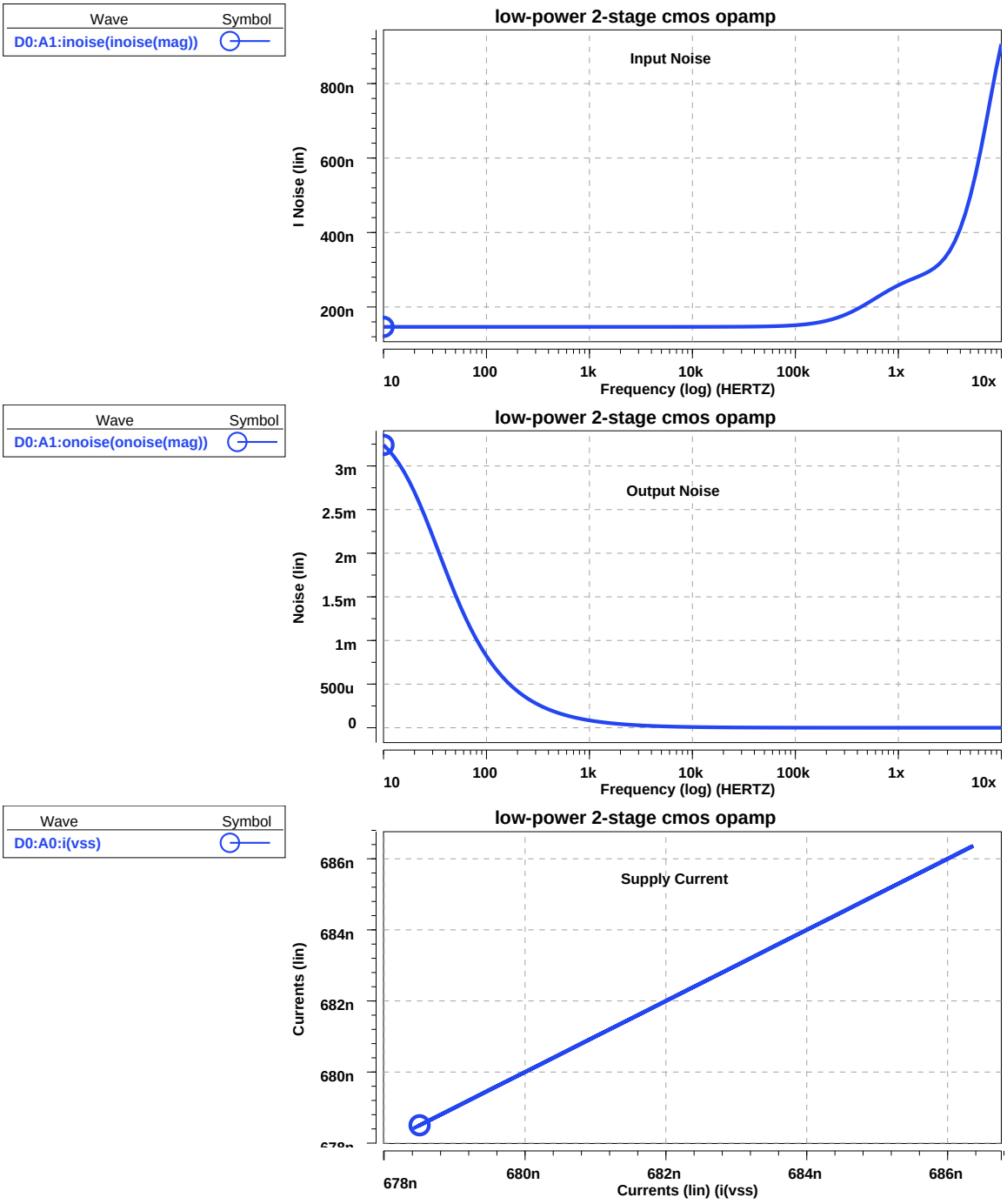


Figure 3: AMP1D_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

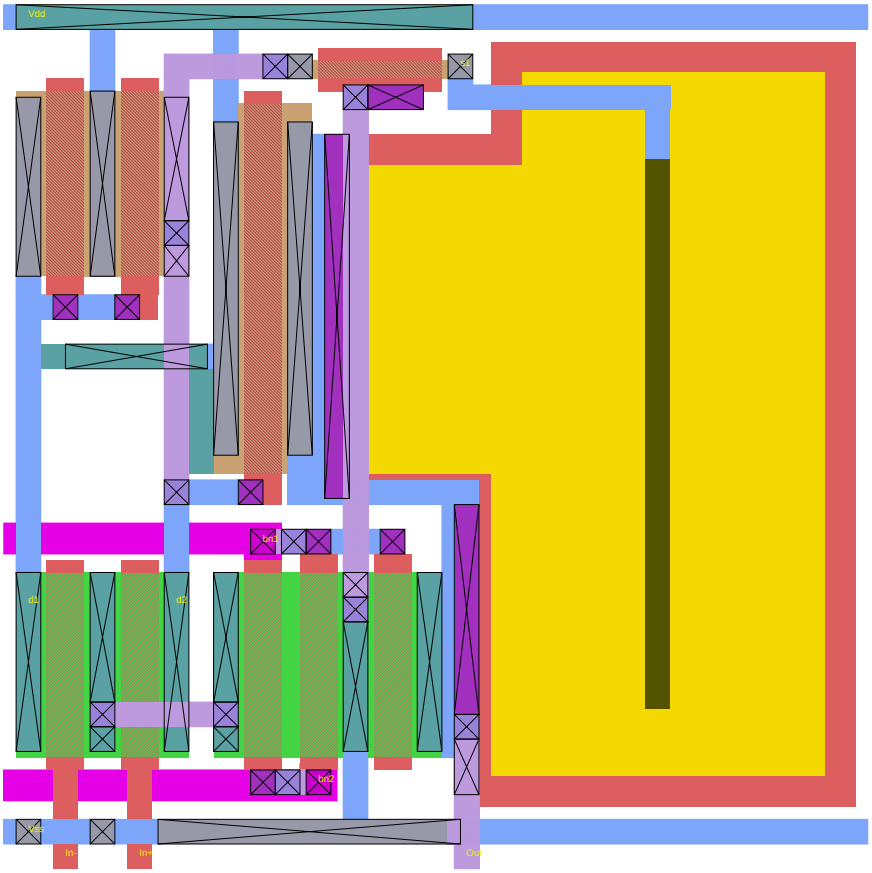


Figure 4: AMP1D_50 Magic Layout 0.5$\mu$m Process