AMP1N1_50 Amplifier

Dr. Godi Fischer
Department of Electrical Engineering
University of Rhode Island
fischer@ele.uri.edu

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Two−Stage CMOS Amplifier

(Amp1n_50)

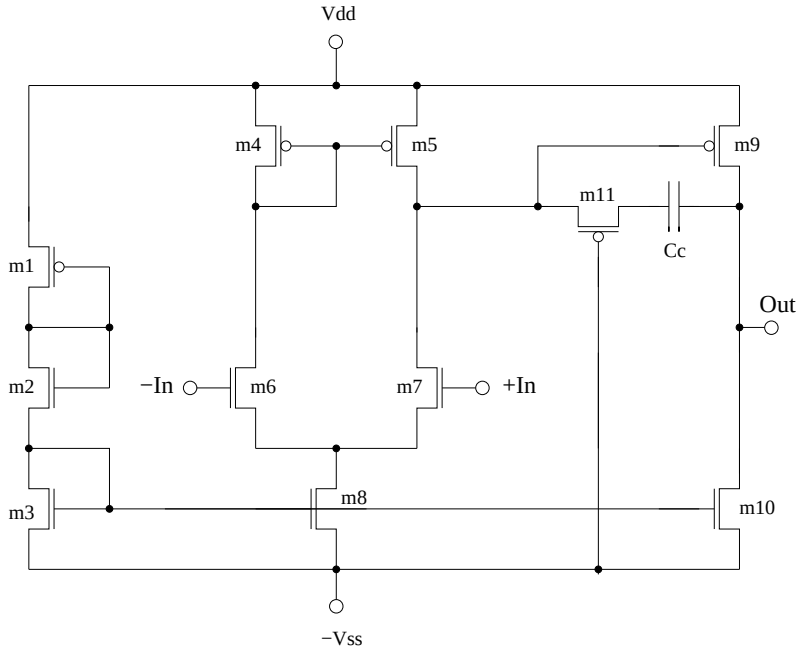

Figure 1: Schematic of the AMP1N1_50

Parameter	Simulated Value
Voltage Swing	± 2.2V
Open Loop Gain	82dB
Gain Bandwidth	32MHz
Phase Margin	45°
Slew Rate @ C_l=10pF	$25\frac{V}{\mu s}$
CMRR @ DC	87dB
CMRR @ AC 100KHz	84dB
PSRR+ @ DC	88dB
PSRR+ @ AC 100KHz	59dB
PSRR- @ DC	93dB
PSRR- @ AC 100KHz	68dB
Power Supply Rails	± 2.5V
$I_{V_{ss}}$	.704mA

Table 1: **Various Parameters of the AMP1N1_50 from Simulation**

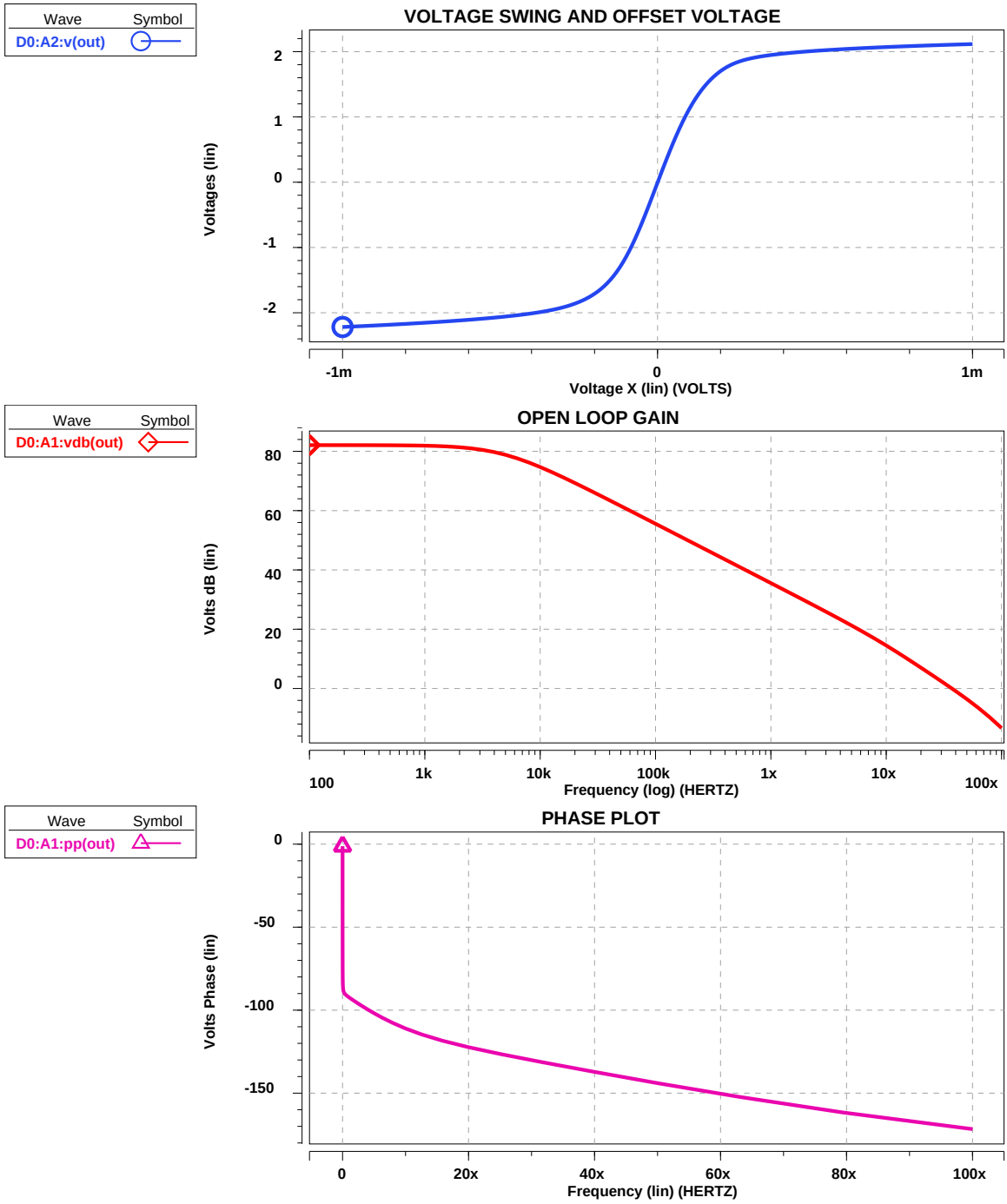

Figure 2: AMP1N1_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

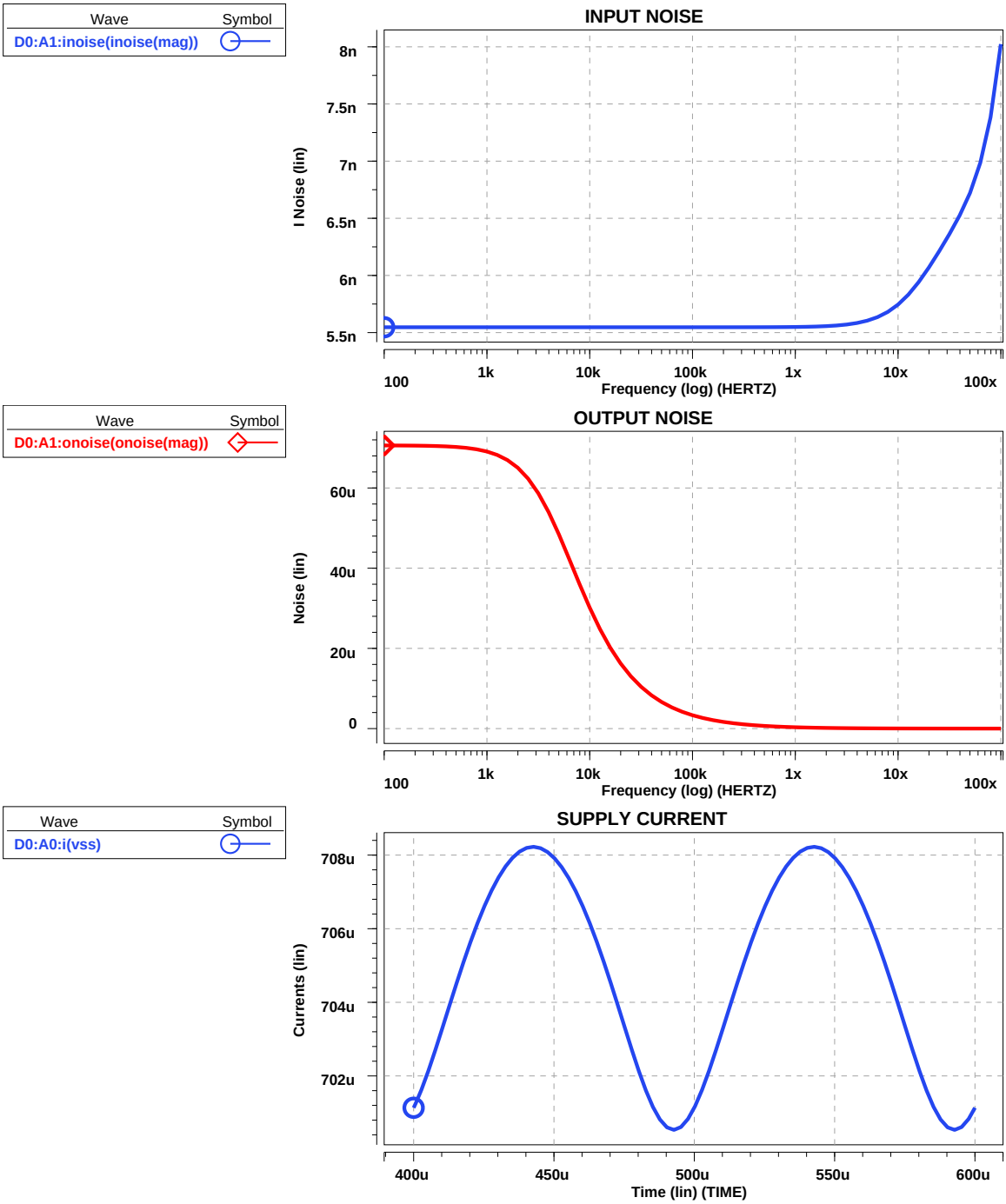

Figure 3: AMP1N1_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

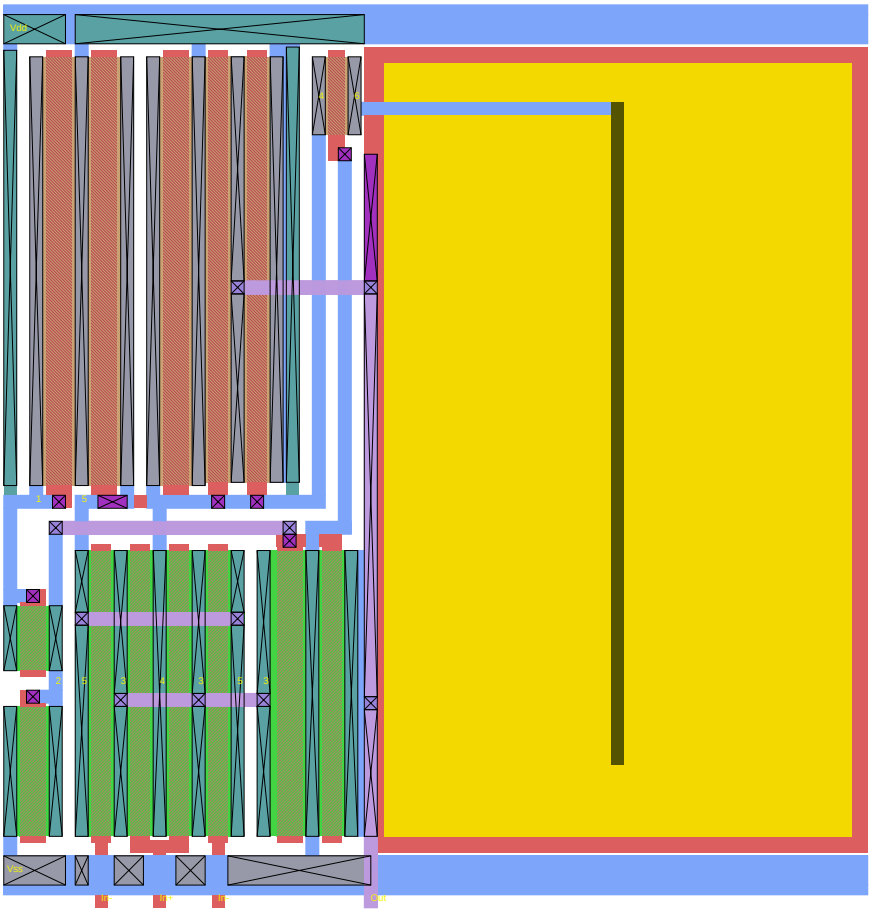

Figure 4: AMP1N1_50 Magic Layout 0.5μm Process