AMP1P_50 Amplifier

Dr. Godi Fischer
Department of Electrical Engineering
University of Rhode Island
fischer@ele.uri.edu

May 1, 2002

Two−Stage CMOS Amplifier

(Amp1n_50)

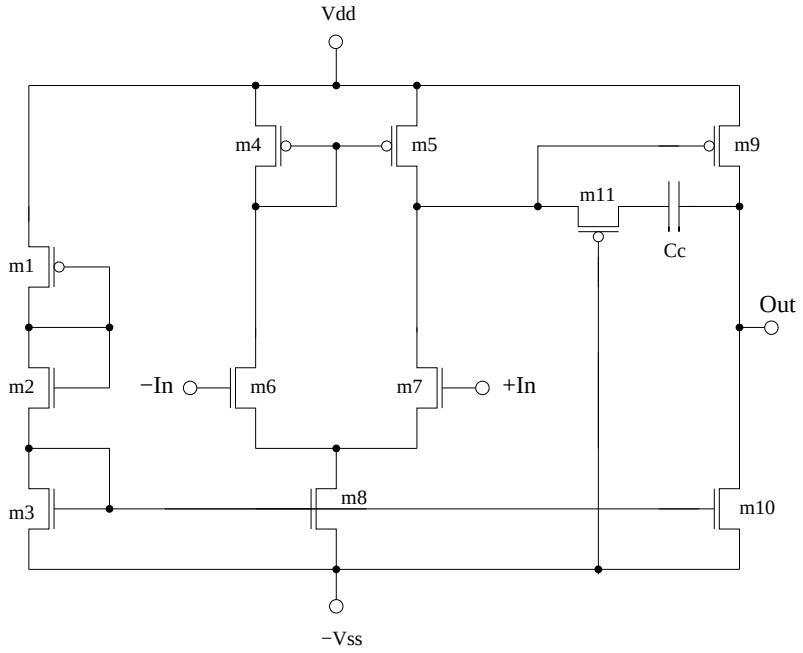

Figure 1: Schematic of the AMP1P_50

Parameter	Simulated Value
Voltage Swing	± 2.4V
Open Loop Gain	80dB
Gain Bandwidth	25.11MHz
Phase Margin	46°
Slew Rate @ C_l=10pF	$25\frac{V}{\mu s}$
CMRR @ DC	84dB
CMRR @ AC 100KHz	84dB
PSRR+ @ DC	89dB
PSRR+ @ AC 100KHz	59dB
PSRR- @ DC	113dB
PSRR- @ AC 100KHz	69dB
Power Supply Rails	± 2.5V
$I_{V_{ss}}$	.574mA

Table 1: **Various Parameters of the AMP1P_50 from Simulation**

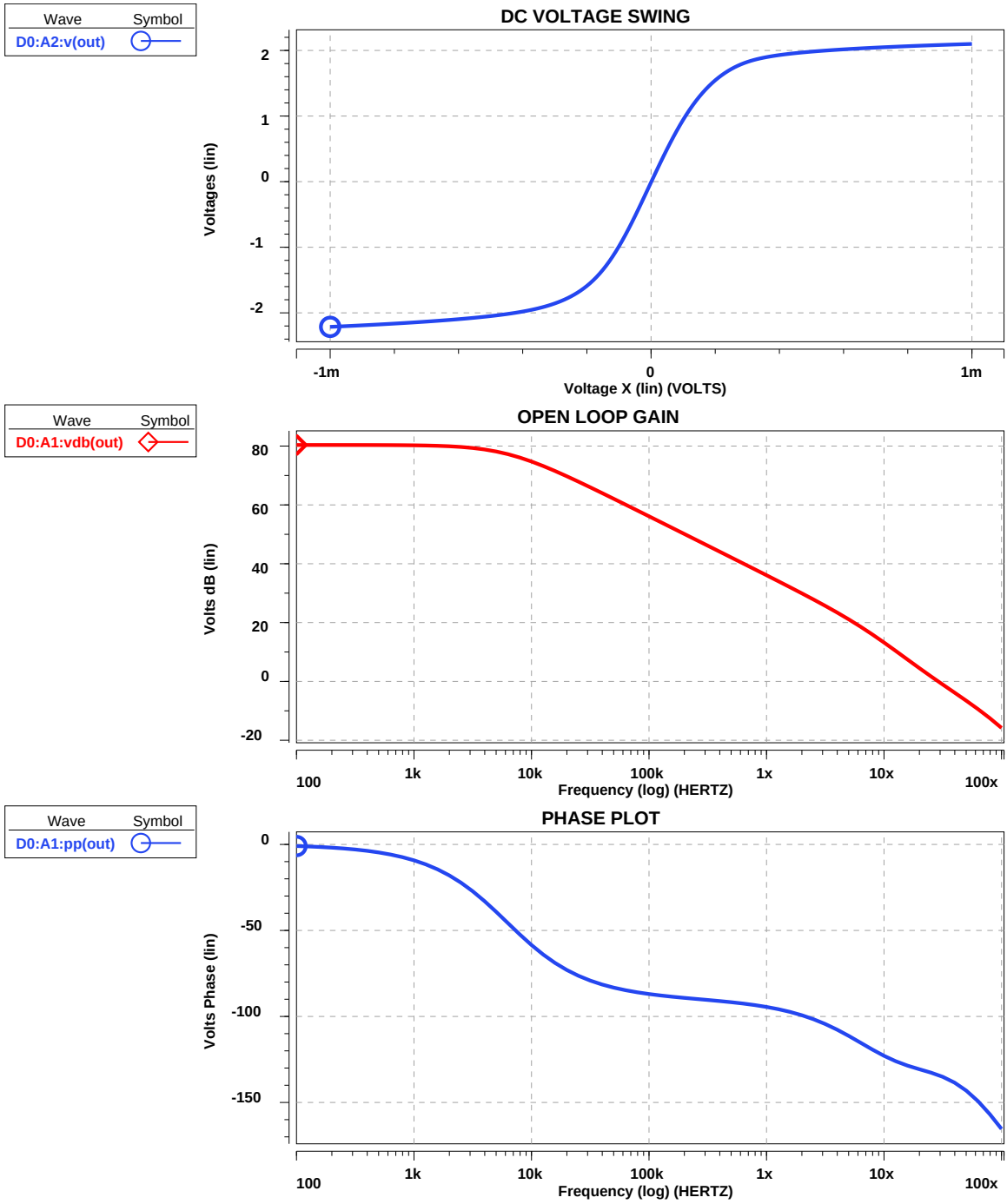

Figure 2: AMP1P_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

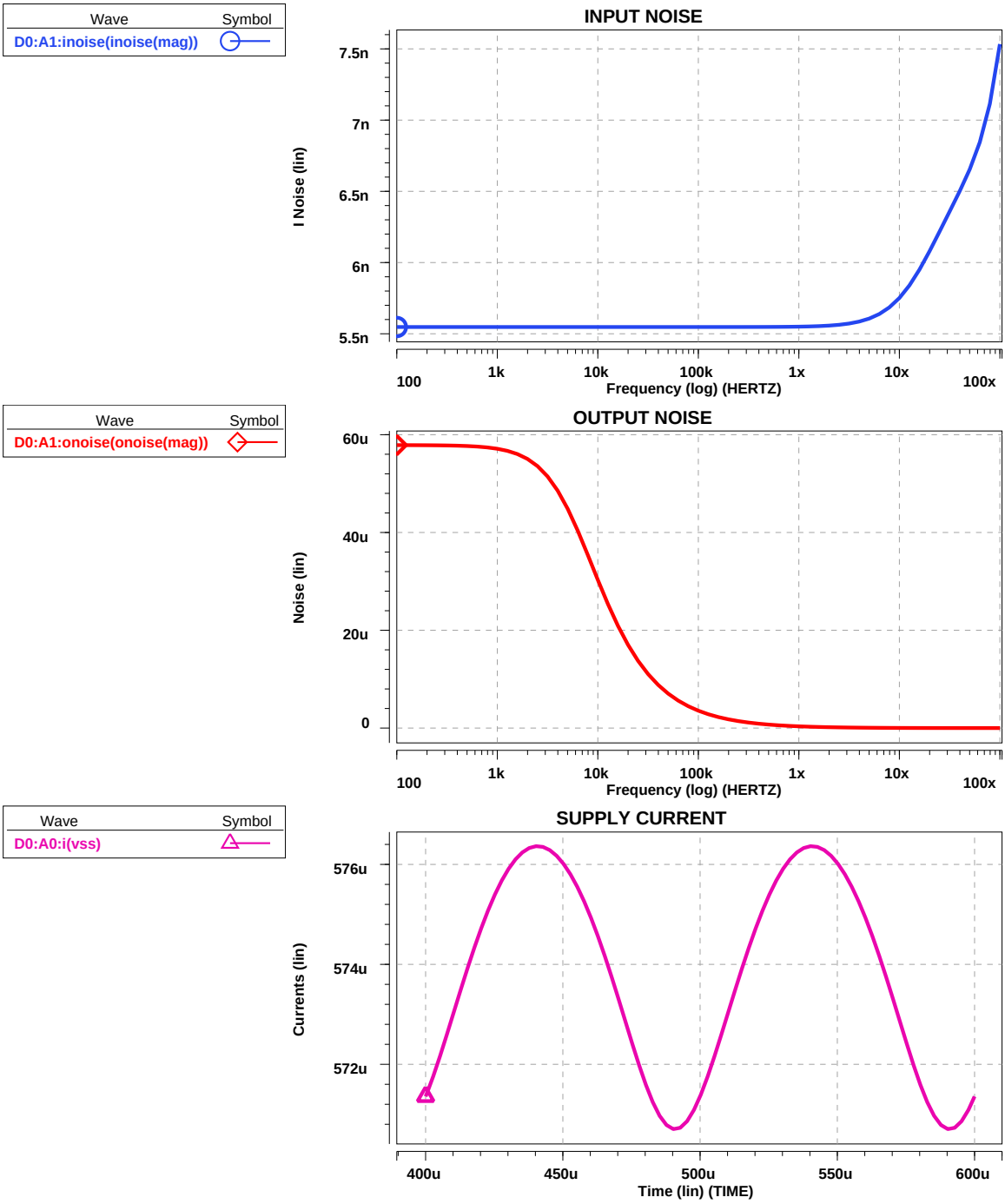

Figure 3: AMP1P_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

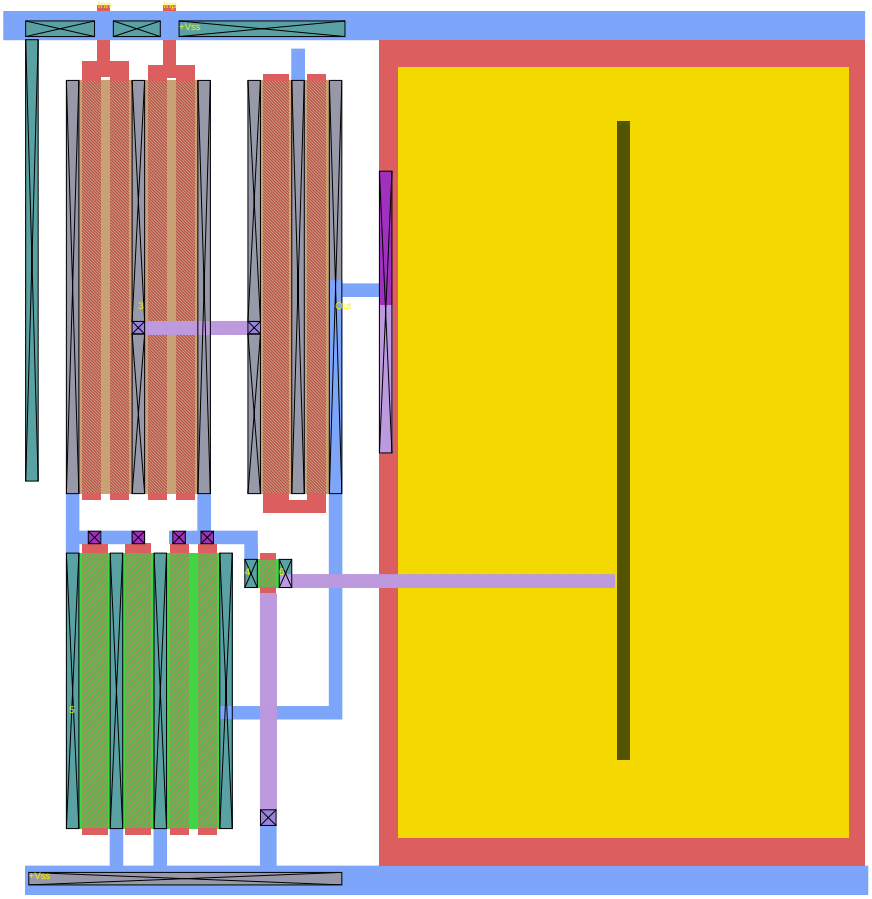

Figure 4: AMP1P1_50 Magic Layout 0.5μm Process