AMP2N2_50 Amplifier

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Two−Stage CMOS Cascode Amplifier

(Amp2n_50)

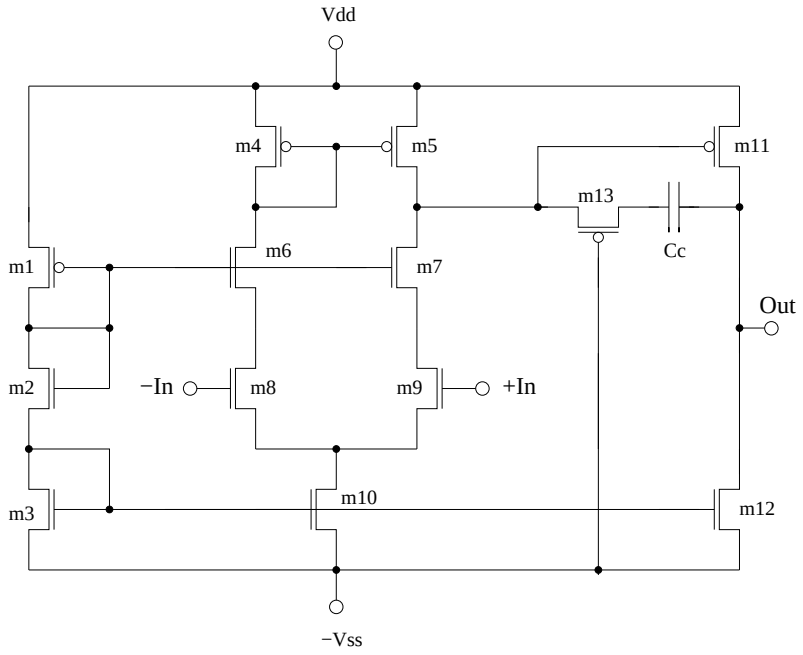

Figure 1: Schematic of the AMP2N2_50

Parameter	Simulated Value
Voltage Swing	$\pm$ 2.4V
Open Loop Gain	90dB
Gain Bandwidth	40MHz
Phase Margin	42.9^o
Slew Rate @ C_l=10pF	$33.34\frac{V}{\mu s}$
CMRR @ DC	95dB
CMRR @ AC 100KHz	95dB
PSRR+ @ DC	97dB
PSRR+ @ AC 100KHz	58.67dB
PSRR- @ DC	116dB
PSRR- @ AC 100KHz	68dB
Power Supply Rails	$\pm$ 2.5V
$I_{V_{ss}}$	.575mA

Table 1: **Various Parameters of the AMP2N2_50 from Simulation**

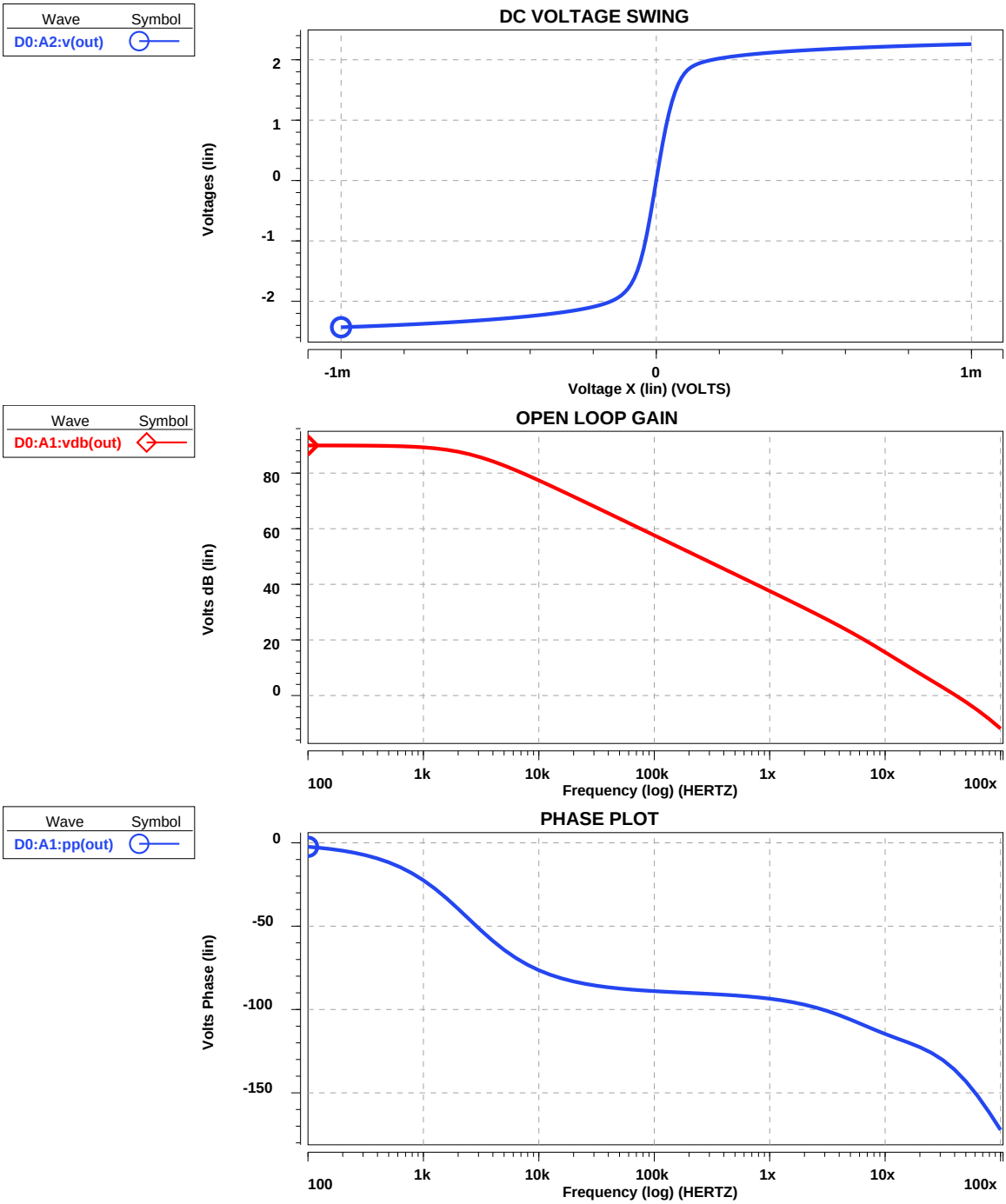

Figure 2: AMP2N2_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

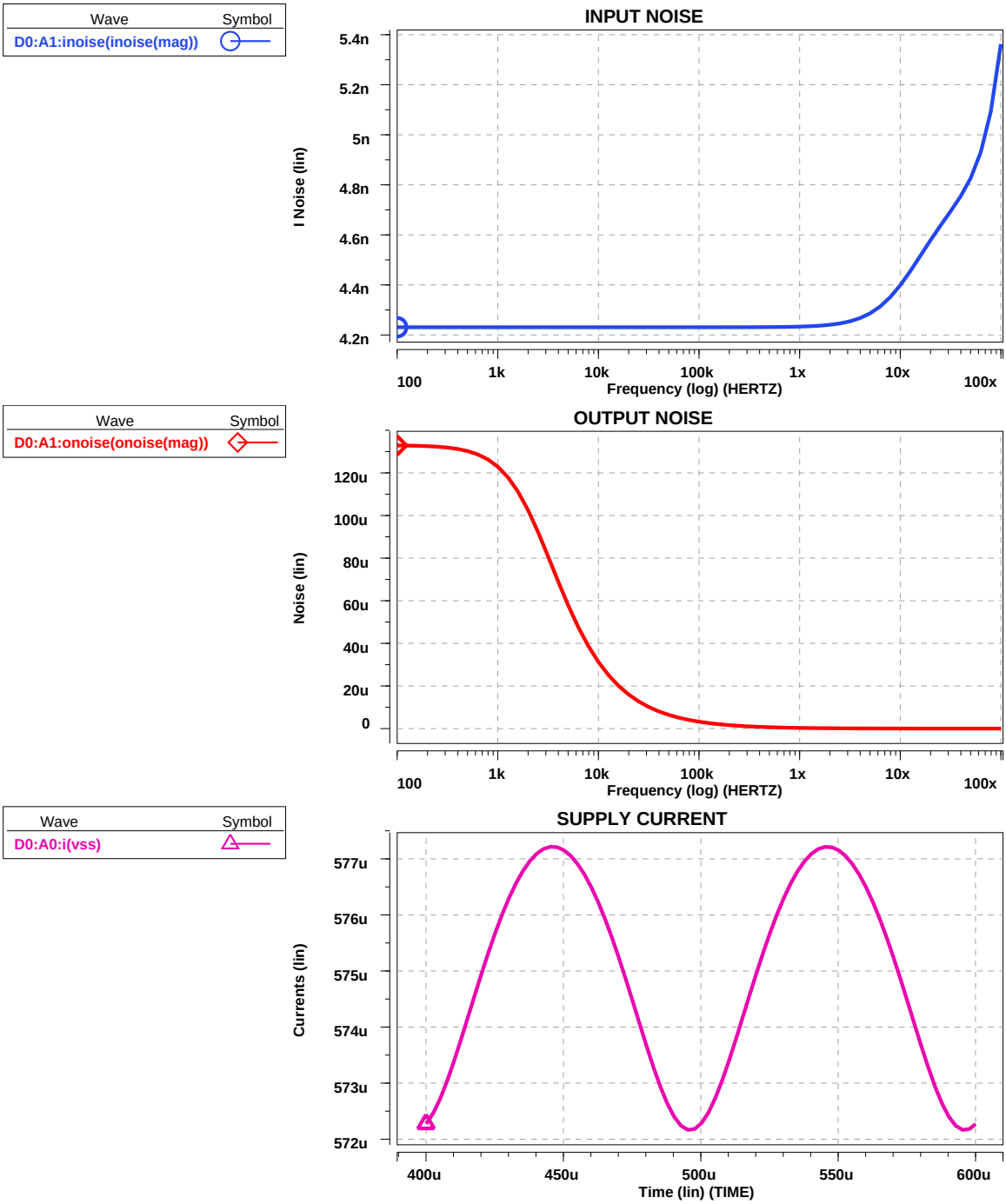

Figure 3: AMP2N2_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

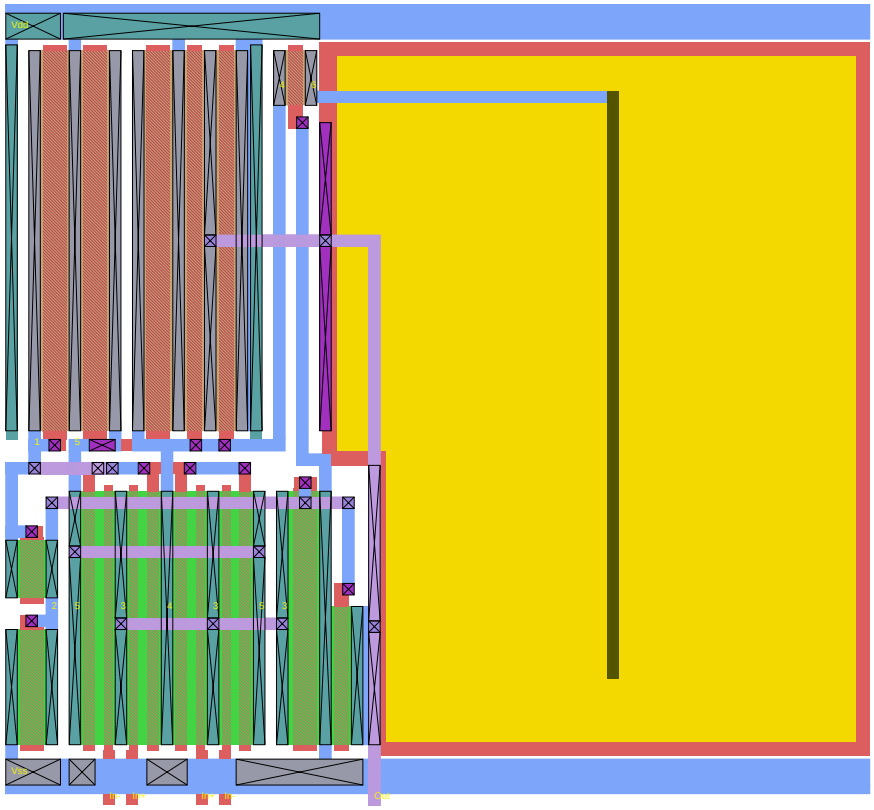

Figure 4: AMP2N2_50 Magic Layout 0.5μm Process