AMP2N3_50 Amplifier

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Two−Stage CMOS Cascode Amplifier

(Amp2n_50)

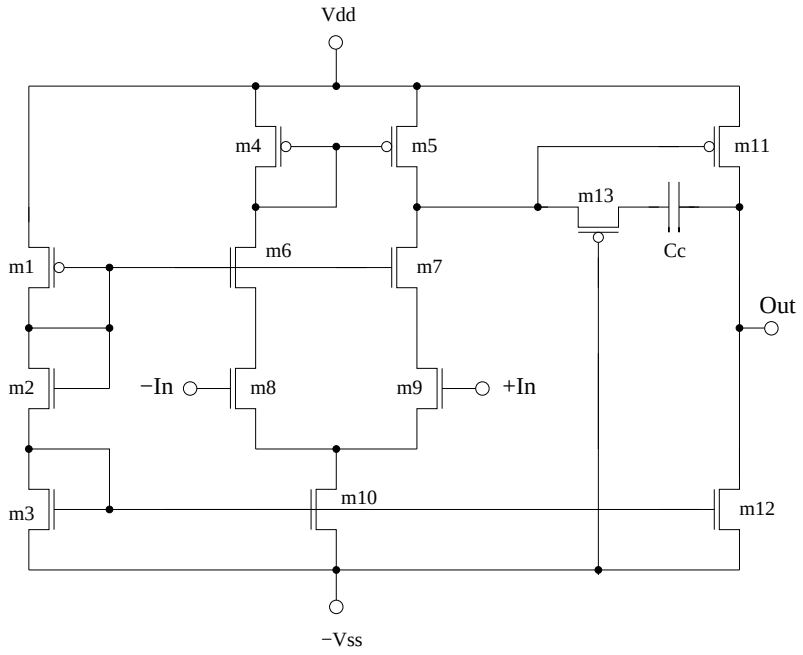

Figure 1: Schematic of the AMP2N3_50

Parameter	Simulated Value
Voltage Swing	$\pm$ 2.4V
Open Loop Gain	88.5dB
Gain Bandwidth	29MHz
Phase Margin	47^o
Slew Rate @ C_l=10pF	$28.57\frac{V}{\mu s}$
CMRR @ DC	93.5dB
CMRR @ AC 100KHz	93dB
PSRR+ @ DC	97.5dB
PSRR+ @ AC 100KHz	59dB
PSRR- @ DC	117.5dB
PSRR- @ AC 100KHz	68dB
Power Supply Rails	$\pm$ 2.5V
$I_{V_{ss}}$	.574mA

Table 1: **Various Parameters of the AMP2N3_50 from Simulation**

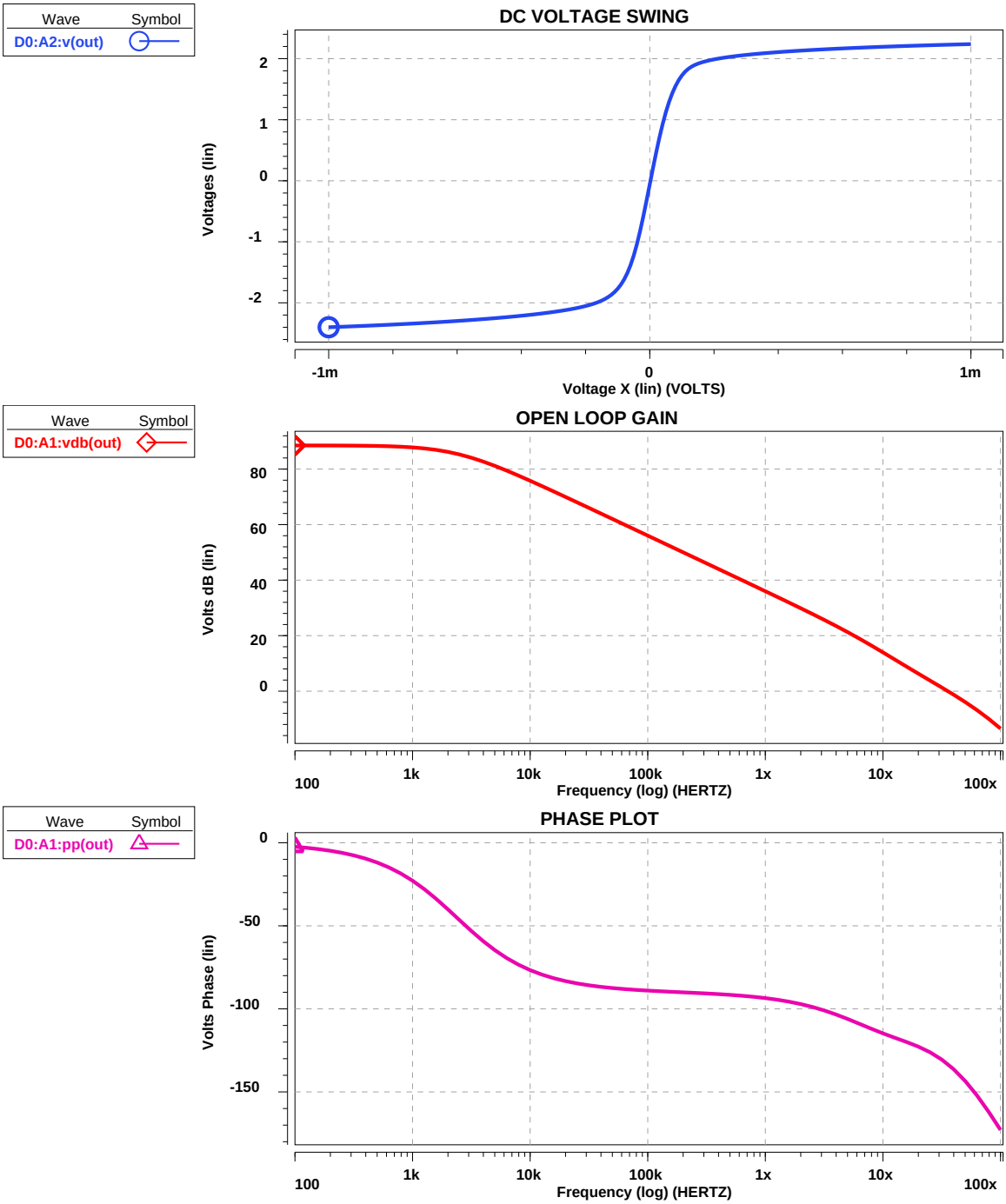

Figure 2: AMP2N3_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

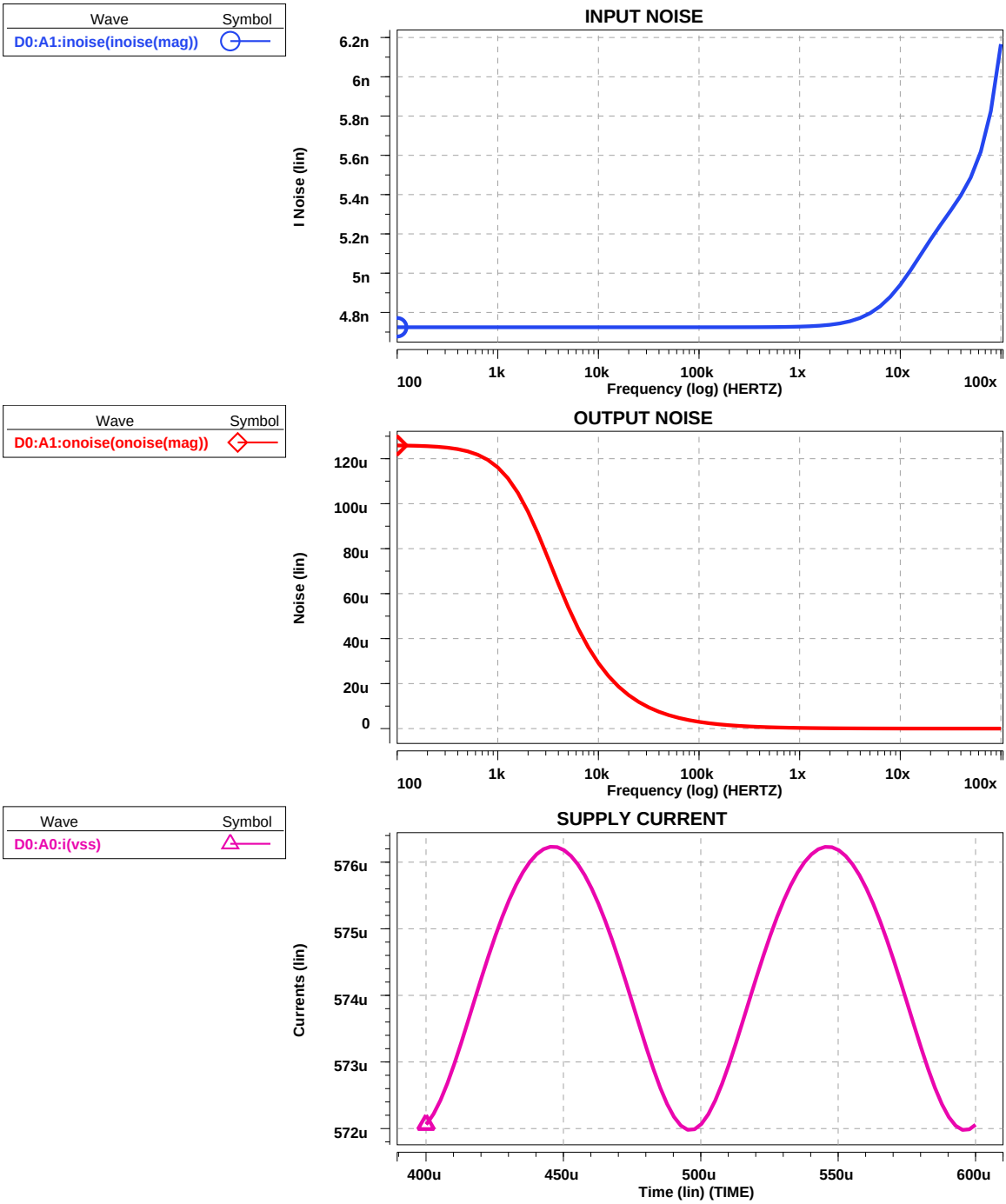

Figure 3: AMP2N3_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

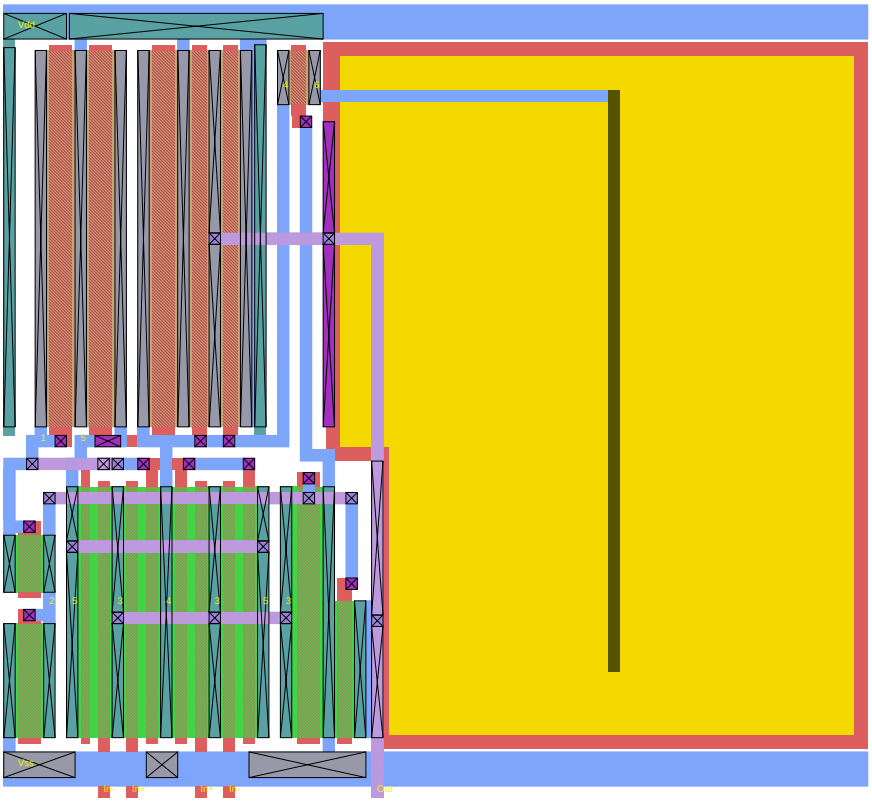

Figure 4: AMP2N3_50 Magic Layout 0.5μm Process