

# OTA1A\_50 Amplifier

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# CMOS Operational Transconductance Amplifier

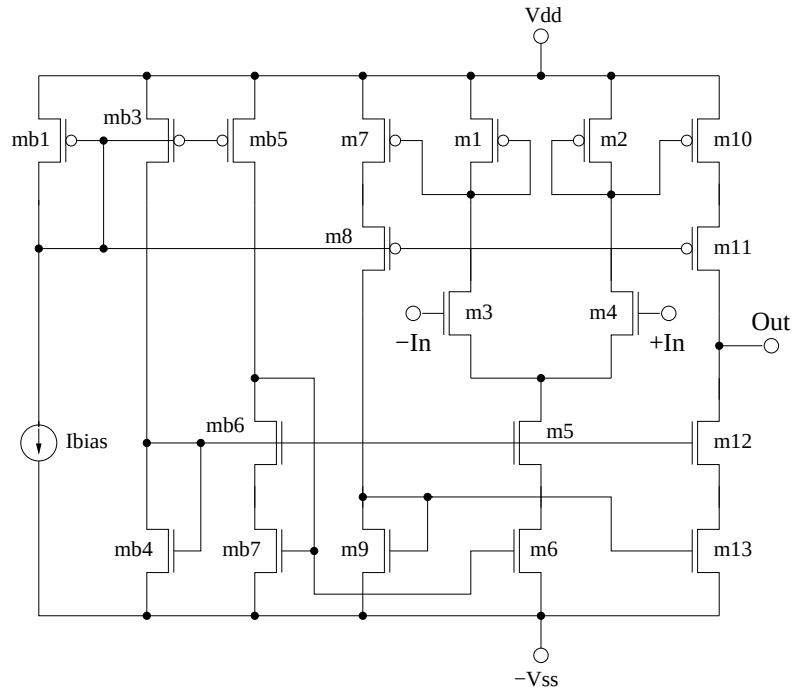


Figure 1: Schematic of the OTA1A\_50

| Parameter                    | Simulated Value                 |
|------------------------------|---------------------------------|
| Voltage Swing                | $\pm 1.2\text{V}$               |
| Open Loop Gain               | 78.319dB                        |
| Gain Bandwidth               | 5.63MHz                         |
| Phase Margin                 | $79^\circ$                      |
| Slew Rate @ $C_l=5\text{pF}$ | $3\frac{\text{V}}{\mu\text{s}}$ |
| CMRR @ DC                    | 129.6dB                         |
| CMRR @ AC 100KHz             | 108dB                           |
| PSRR+ @ DC                   | 98.319dB                        |
| PSRR+ @ AC 100KHz            | 84dB                            |
| PSRR- @ DC                   | 79dB                            |
| PSRR- @ AC 100KHz            | 61dB                            |
| Power Supply Rails           | $\pm 1.5\text{V}$               |
| $I_{V_{ss}}$                 | $41.49\mu\text{A}$              |

Table 1: **Various Parameters of the OTA1A\_50 from Simulation**

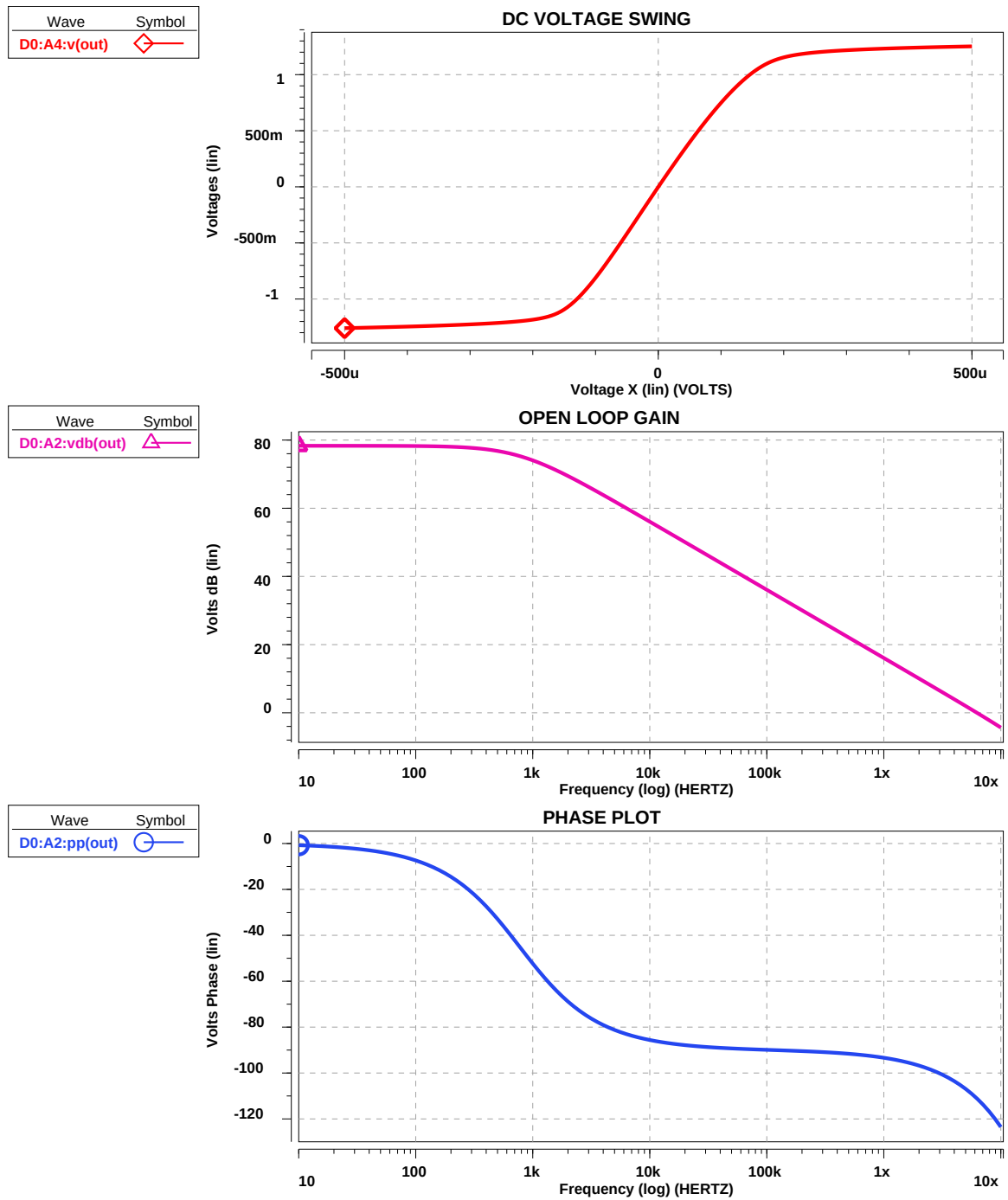
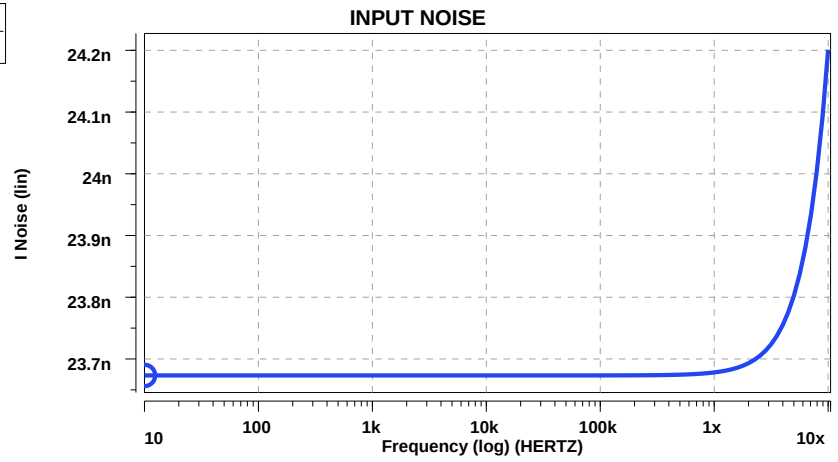
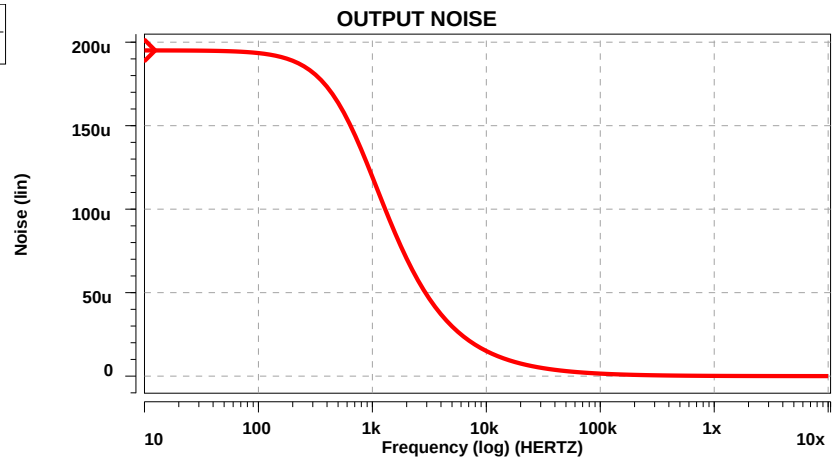


Figure 2: OTA1A\_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

| Wave                      | Symbol                                                                            |
|---------------------------|-----------------------------------------------------------------------------------|
| D0:A2:inoise(inoise(mag)) |  |



| Wave                      | Symbol                                                                            |
|---------------------------|-----------------------------------------------------------------------------------|
| D0:A2:onoise(onoise(mag)) |  |



| Wave         | Symbol                                                                              |
|--------------|-------------------------------------------------------------------------------------|
| D0:A0:i(vss) |  |

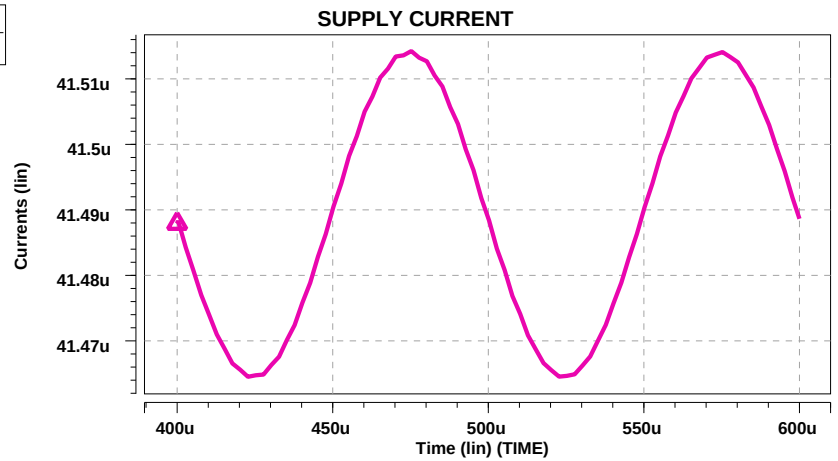


Figure 3: OTA1A\_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

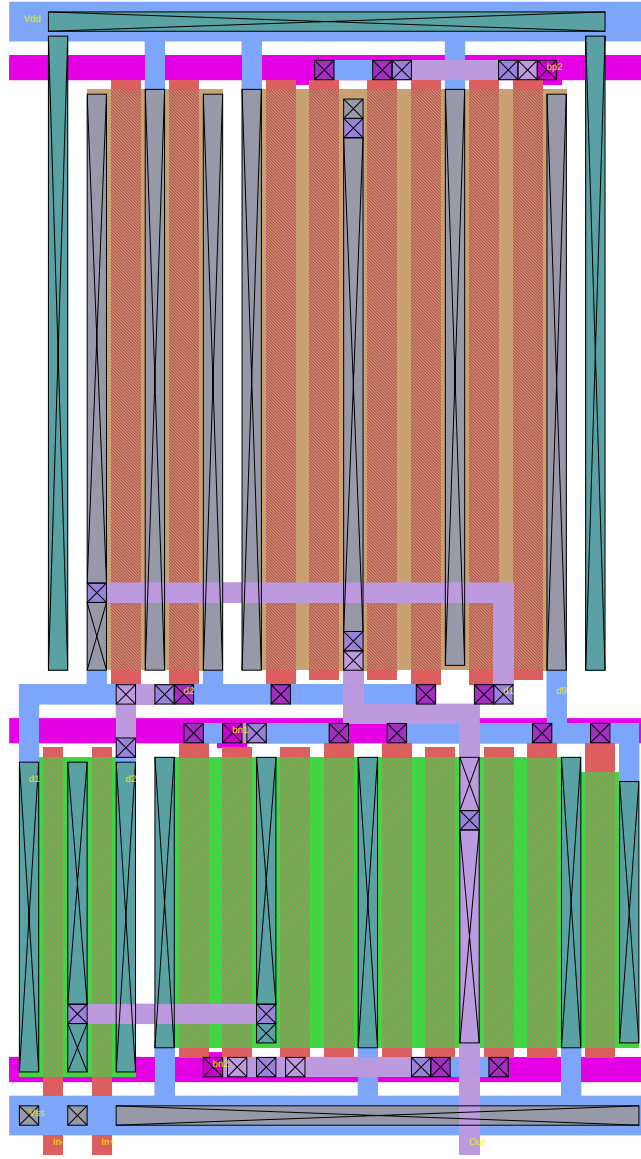


Figure 4: OTA1A\_50 Magic Layout 0.5 $\mu$ m Process