OTA1B_50 Amplifier

Dr. Godi Fischer
Department of Electrical Engineering
University of Rhode Island
fischer@ele.uri.edu

April 28, 2002

CMOS Operational Transconductance Amplifier

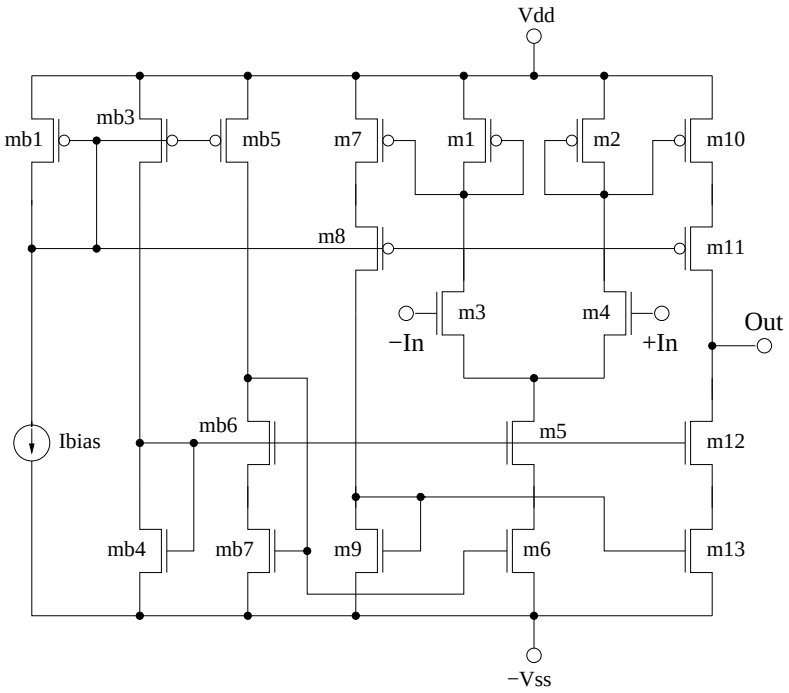

Figure 1: Schematic of the OTA1B_50

Parameter	Simulated Value
Voltage Swing	$\pm$ 1.4V
Open Loop Gain	76.5dB
Gain Bandwidth	3MHz
Phase Margin	70.9^o
Slew Rate @ C_l=5pF	$1.5\frac{V}{\mu s}$
CMRR @ DC	126dB
CMRR @ AC 100KHz	106dB
PSRR+ @ DC	100dB
PSRR+ @ AC 100KHz	107dB
PSRR- @ DC	76.5dB
PSRR- @ AC 100KHz	62dB
Power Supply Rails	$\pm$ 1.5V
$I_{V_{ss}}$	19.93μA

Table 1: **Various Parameters of the OTA1B_50 from Simulation**

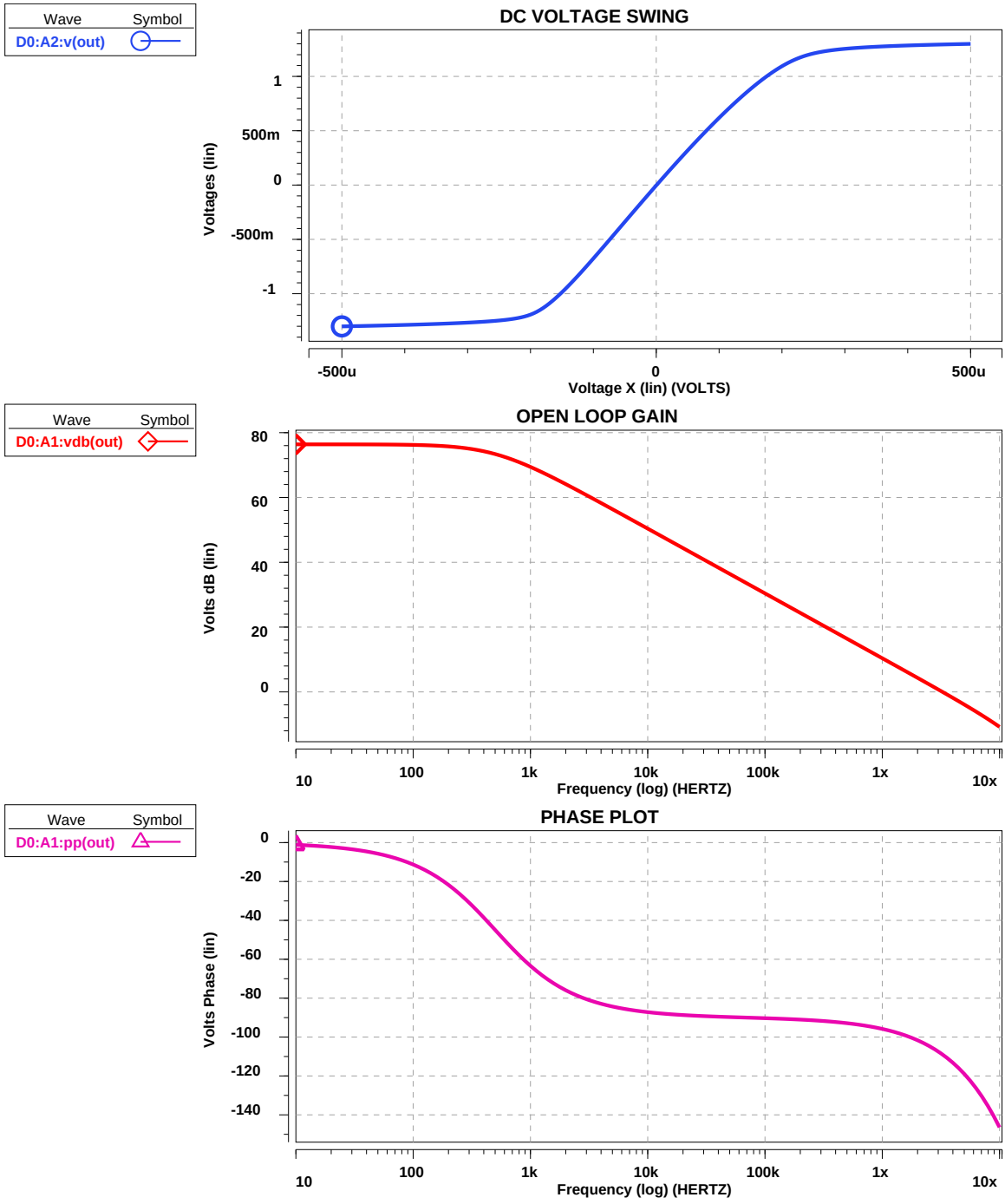

Figure 2: OTA1B_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

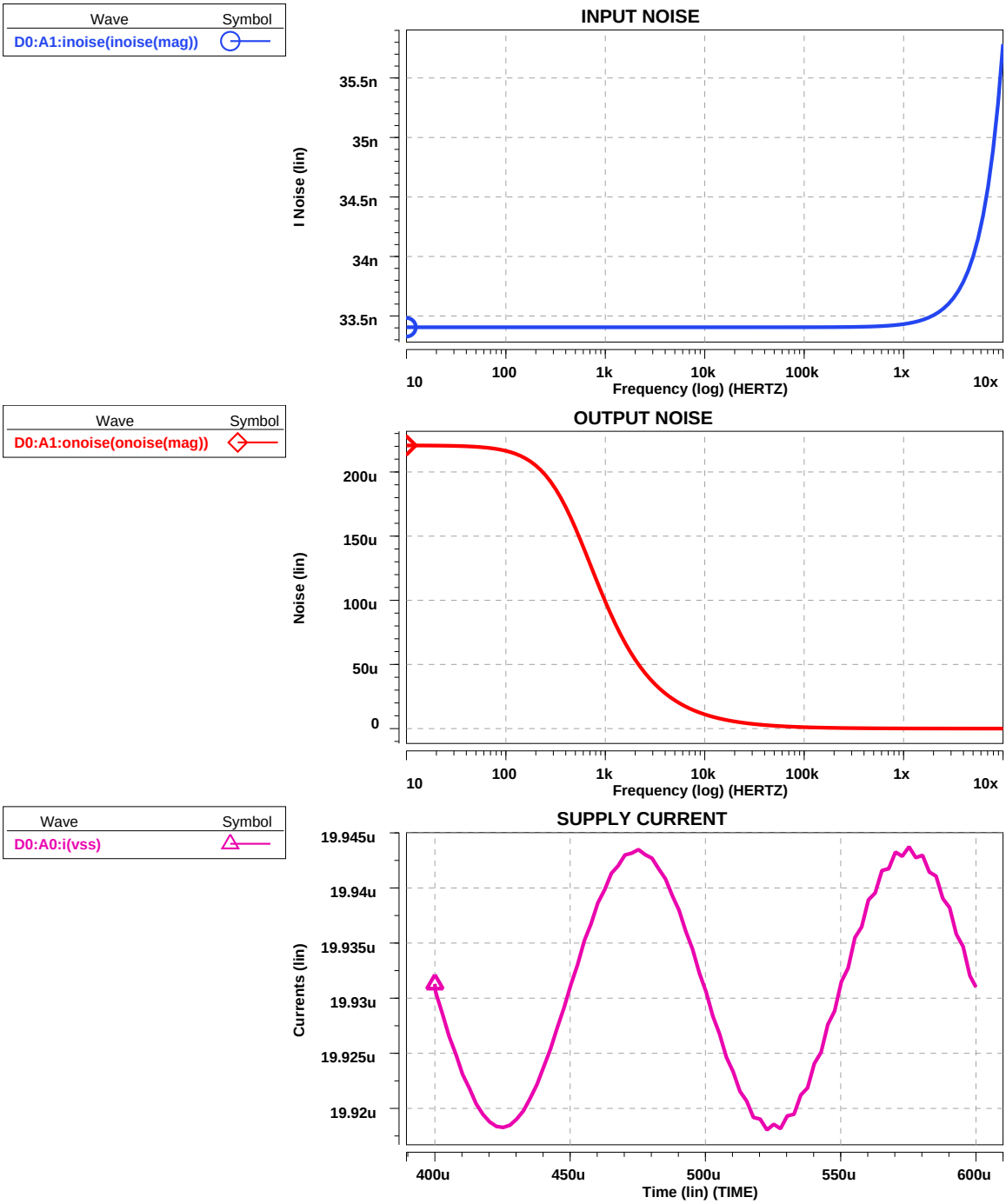

Figure 3: OTA1B_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

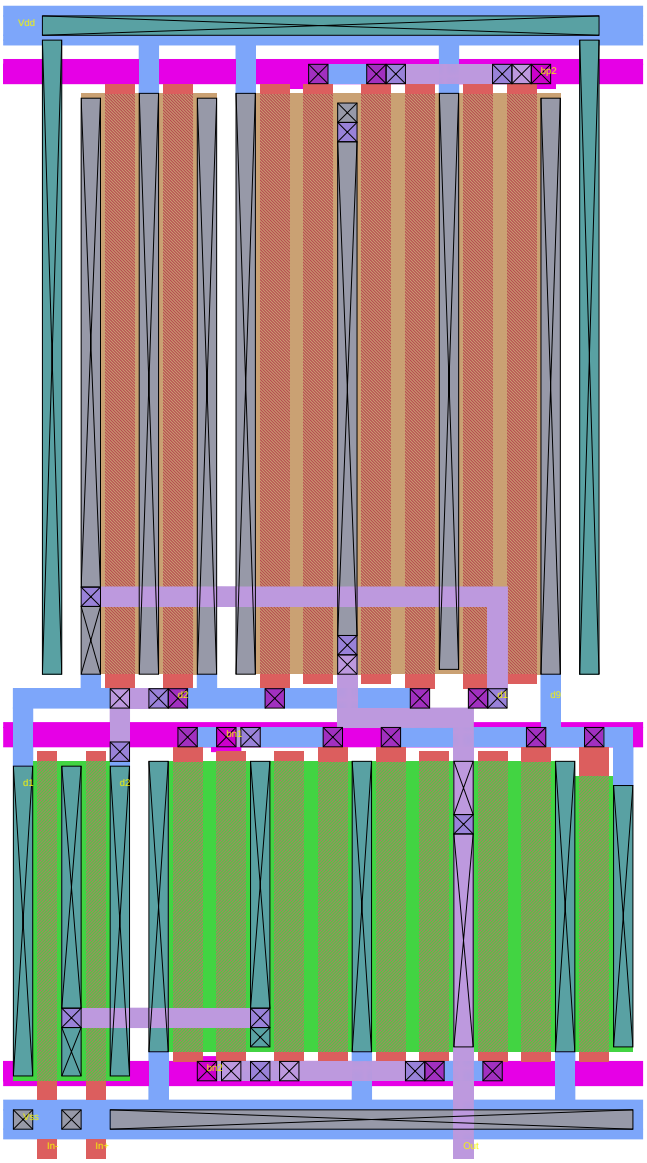

Figure 4: OTA1B_50 Magic Layout 0.5μm Process