OTA1C_50 Amplifier

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CMOS Operational Transconductance Amplifier

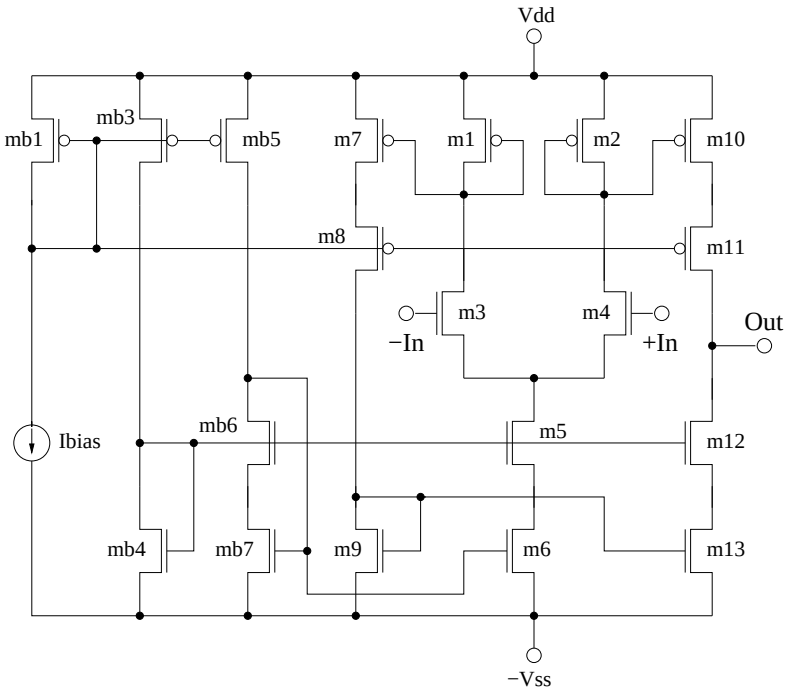

Figure 1: Schematic of the OTA1C_50

Parameter	Simulated Value
Voltage Swing	$\pm$ 1.3V
Open Loop Gain	84.102dB
Gain Bandwidth	750KMHz
Phase Margin	79^o
Slew Rate @ C_l=5pF	$.35\frac{V}{\mu s}$
CMRR @ DC	156dB
CMRR @ AC 100KHz	103dB
PSRR+ @ DC	127dB
PSRR+ @ AC 100KHz	88dB
PSRR- @ DC	84dB
PSRR- @ AC 100KHz	55dB
Power Supply Rails	$\pm$ 1.5V
$I_{V_{ss}}$	4.3μA

Table 1: **Various Parameters of the OTA1C_50 from Simulation**

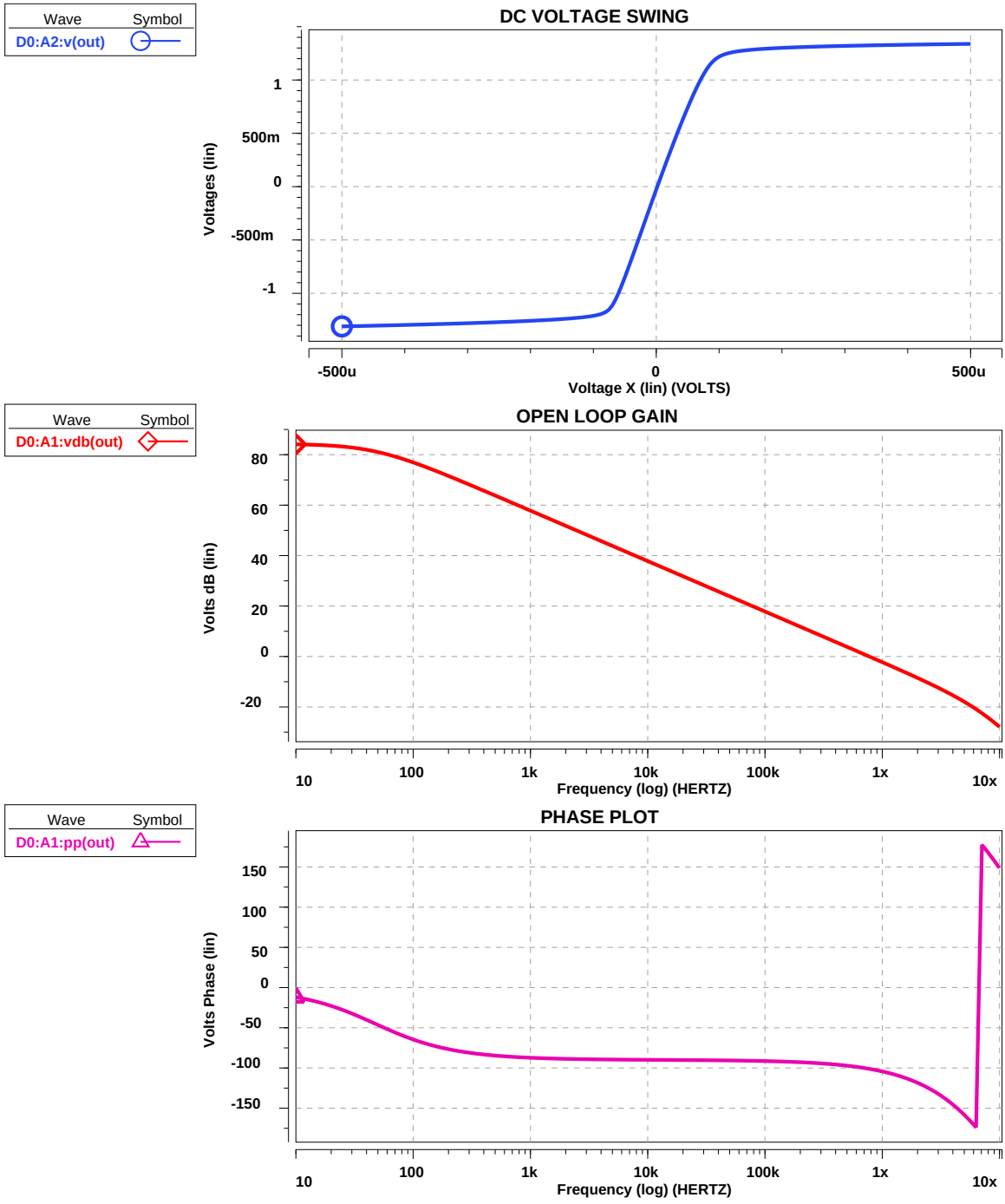

Figure 2: OTA1C_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

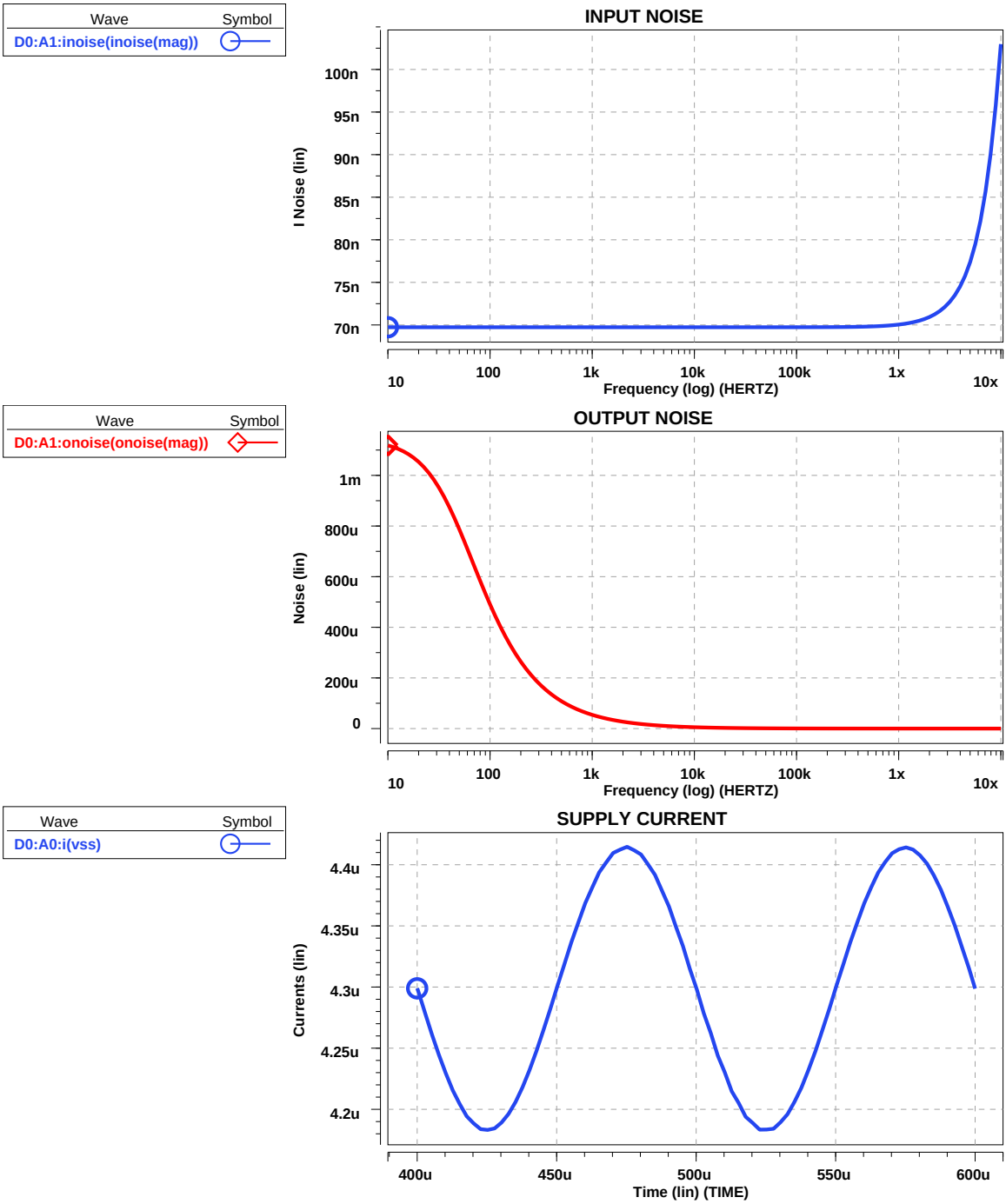

Figure 3: OTA1C_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

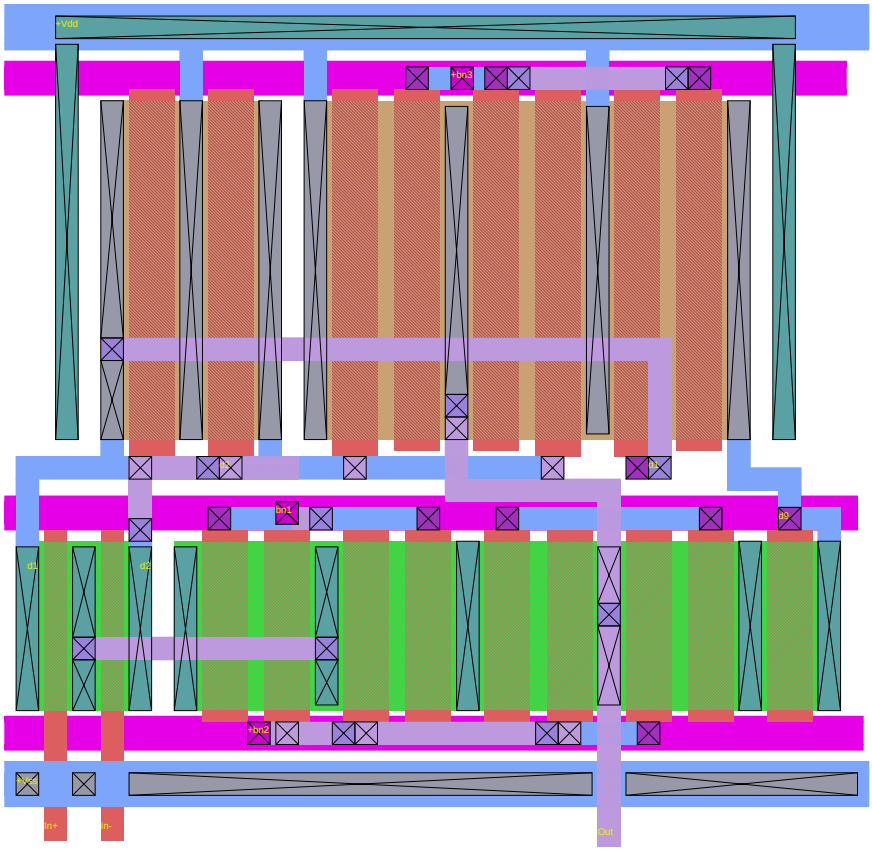

Figure 4: OTA1C_50 Magic Layout 0.5μm Process