OTA1D_50 Amplifier

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CMOS Operational Transconductance Amplifier

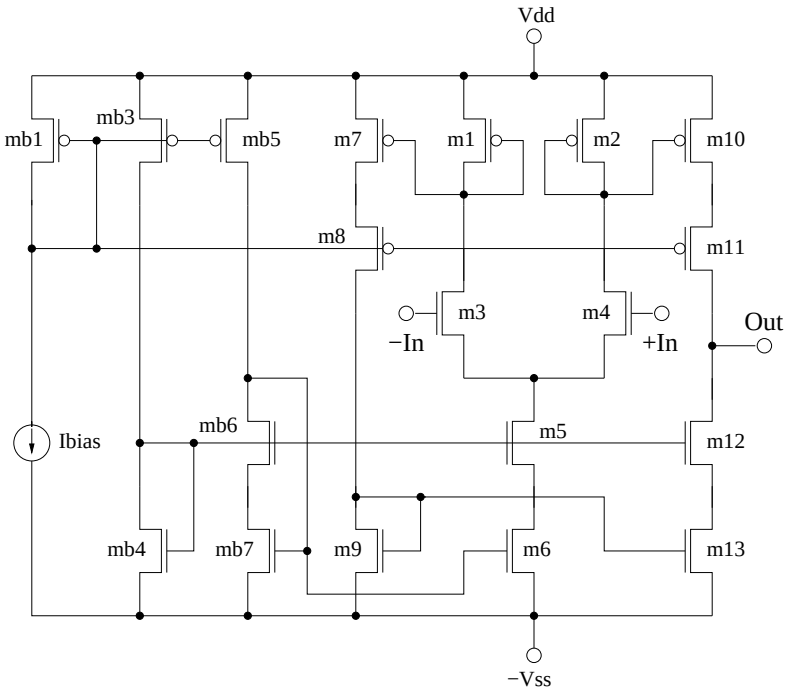

Figure 1: Schematic of the OTA1D_50

Parameter	Simulated Value
Voltage Swing	± V
Open Loop Gain	80dB
Gain Bandwidth	330KMHz
Phase Margin	77.1^o
Slew Rate @ C_l=2.5pF	$0.17\frac{V}{\mu s}$
CMRR @ DC	134dB
CMRR @ AC 100KHz	82dB
PSRR+ @ DC	99dB
PSRR+ @ AC 100KHz	76dB
PSRR- @ DC	81dB
PSRR- @ AC 100KHz	52dB
Power Supply Rails	± 1.5V
$I_{V_{ss}}$	μA

Table 1: **Various Parameters of the OTA1D_50 from Simulation**

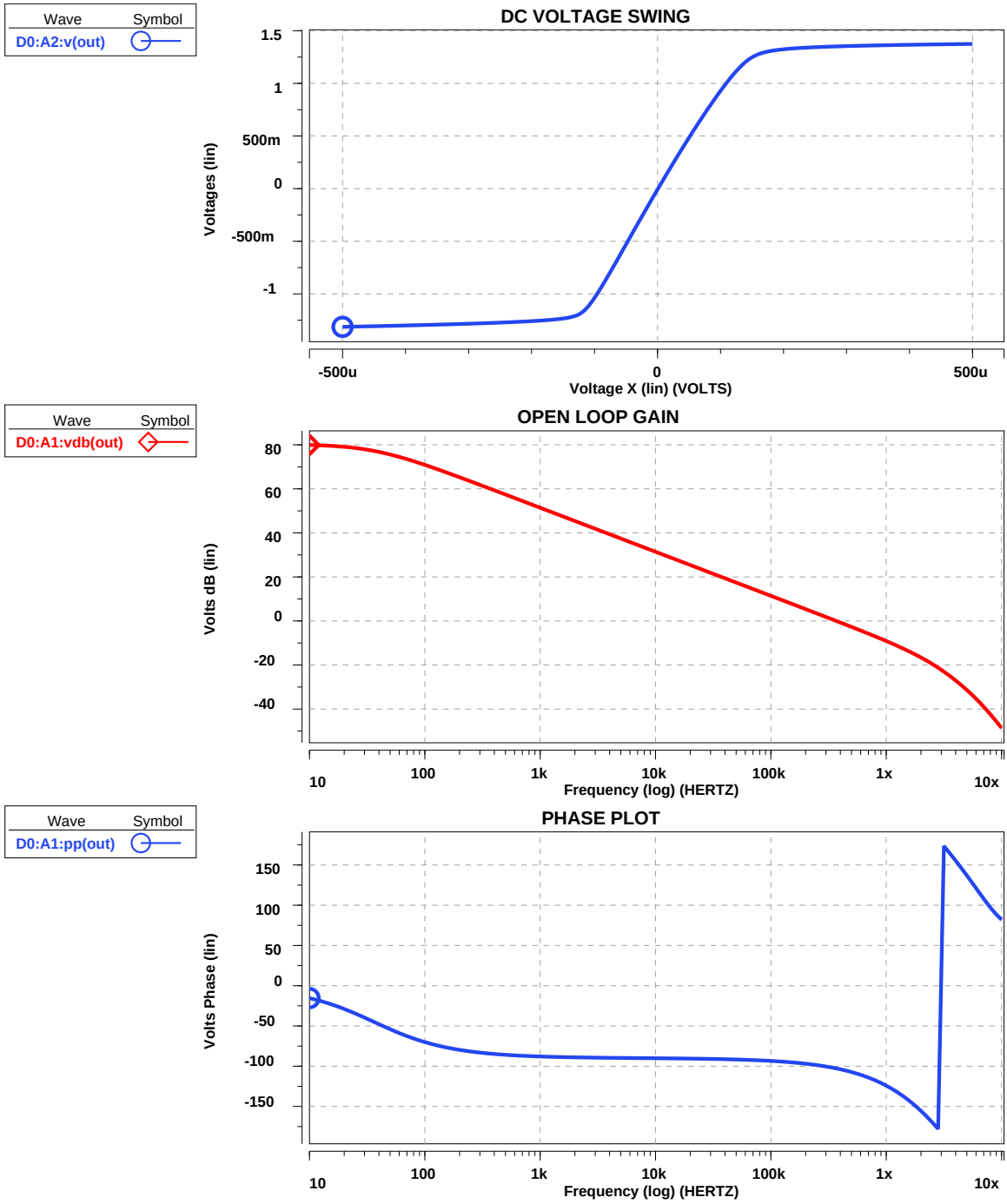

Figure 2: OTA1D_50 Simulations (a) Voltage Swing (b) Gain (c) Phase Plot

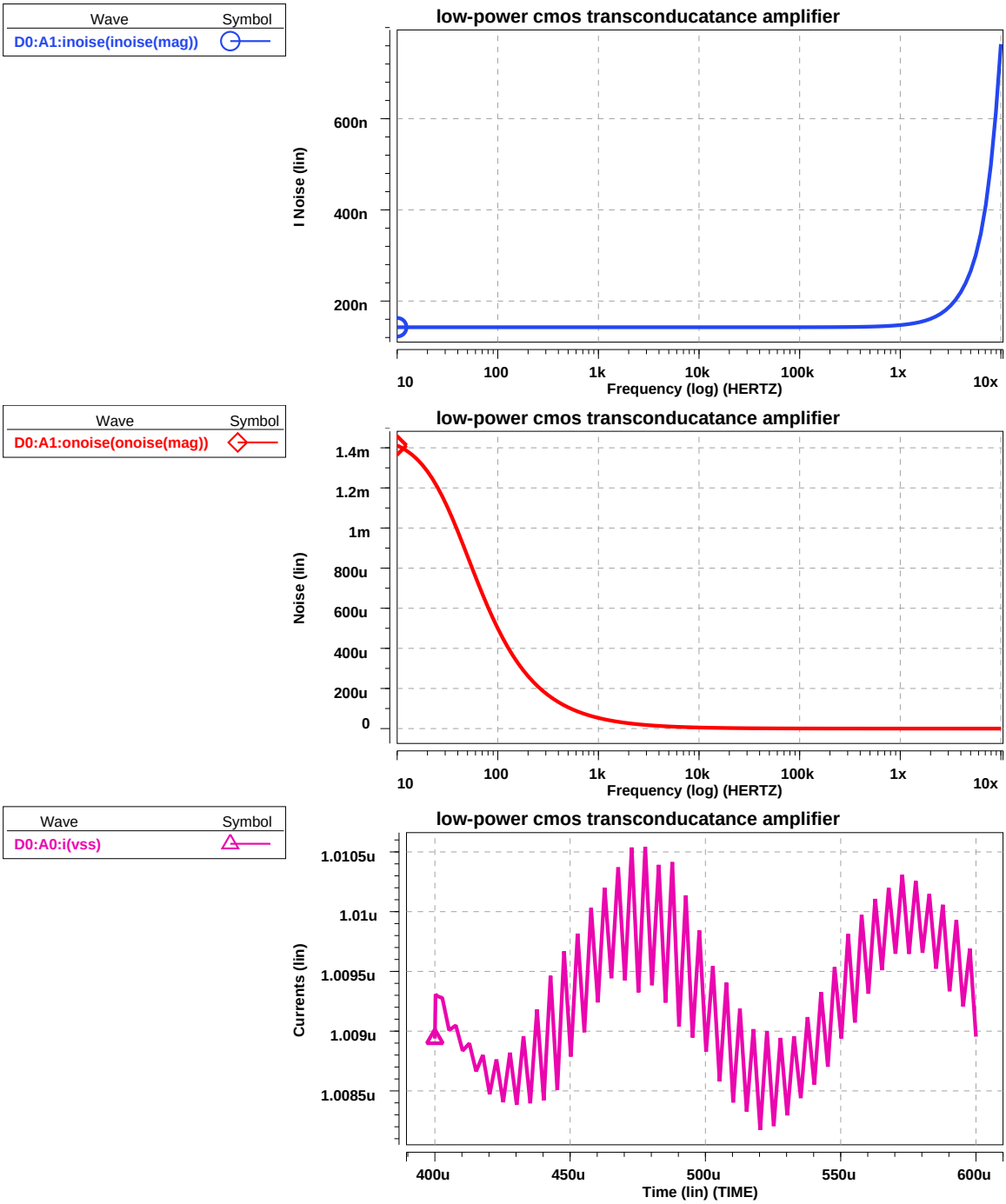

Figure 3: OTA1D_50 Simulations (a) Input Noise (b) Output Noise (c) Supply Current

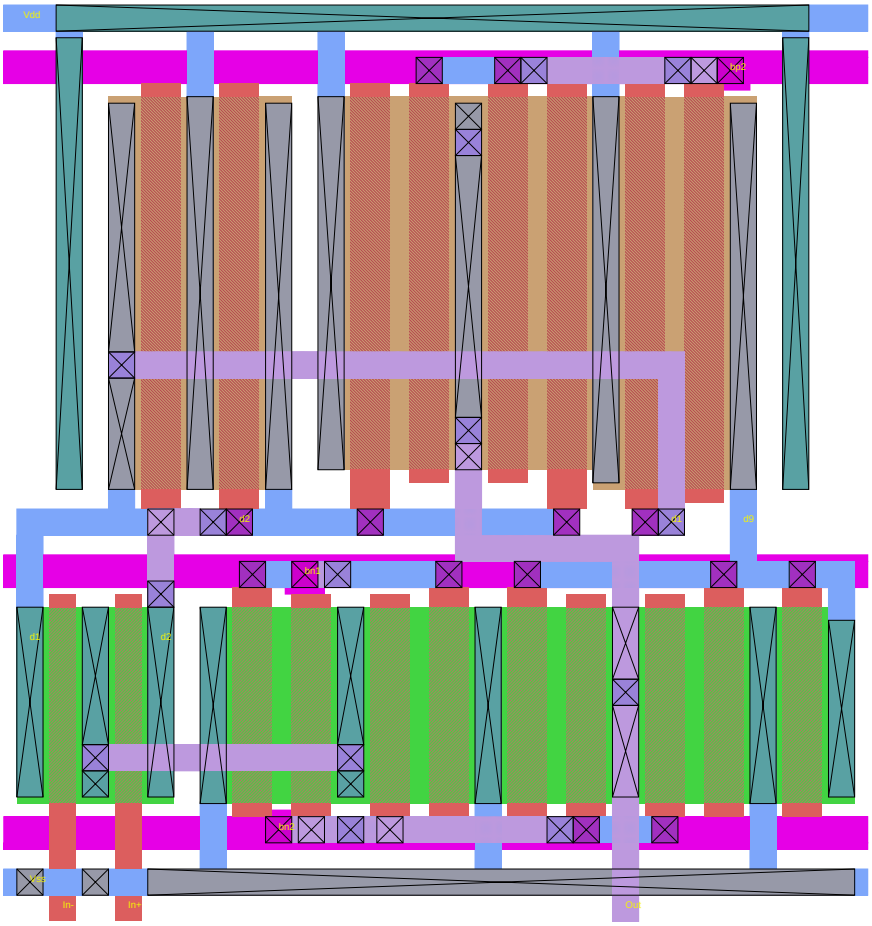

Figure 4: OTA1D_50 Magic Layout 0.5μm Process