Section 4. Power Management

Minimizing Power Consumption of Electronic Devices

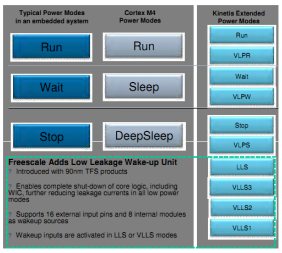
Importance of Low Power Consumption

- Power consumption of computers have become an important issue
- Cost of energy: $14 million electric bill per year for a data center of 30,000 sqft, $4billion a year aggregate
  "What matters most to the computer designers at Google is not speed but power – low power, because data centers can consume as much electricity as a city." – Eric Schmidt, CEO, Google
- Difficult to cool a data center
- Heat generation of power consumption
- Battery life of portable devices
- Environmental impact of power consumption

Power Management Module of K70

- Three primary modes of operation:
  - Run: system works in normal mode
  - Wait: Stops clocks to CPU and memory only
  - Stop: Stops all clocks to the system
- a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory.
- I/O states are held in all modes of operation.
- Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power

Kinetis Power Modes



Mode	Definition
Run	MCU can be run at full speed.
Wait	Allows peripherals to function, while CPU goes to sleep reducing power consumption.
VLP Run	CPU and peripheral clock maximum frequency is restricted. CPU/Platform clock is restricted to 2 MHz. Flash access is restricted to 1 MHz. LVD is off.
VLP Wait	Similar to VLP Run, with CPU in sleep to further reduce power.
Stop	MCU is in static state. Lowest power mode that retains all registers while maintaining LVD protection.
VLP Stop	MCU is in static state with LVD operation off. Lowest power mode with ADC, LPT, RTC, LCD, HSCMP, DAC, and pin interrupts functional.
LL Stop	MCU is in low leakage state retention power mode. LLWU controls wakeup sources including LPT, RTC, LCD, HSCMP, DAC and select pin interrupts.
VLL Stop 3	MCU is placed in a low leakage mode powering down most internal logic. All system RAM contents are retained and I/O states held. LLWU controls wakeup sources including LPT, RTC, LCD, HSCMP, DAC and select pin interrupts.
VLL Stop 2	Similar to VLL Stop 3, with only partial system RAM retention. FlexRAM contents can optionally be retained.
VLL Stop 1	Similar to VLL Stop 3, with only 32 byte register file retention.

Core and System Functions

M4 Core Mode	NVIC	AWIC	LLWU	RAM	Kinetis IDD (typ)
Run	EN	DIS			50 ma @96 M
Run	EN	DIS			1.5 ma
Sleep	EN	DIS			43 ma
Sleep	EN	DIS			1.2 ma
Sleep-Deep	DIS	EN			50 µa
Sleep-Deep	DIS	EN			20 µa
Sleep-Deep	DIS	EN	EN	All	10 µa
Sleep-Deep	DIS	EN	EN	All	6 µa
Sleep-Deep	DIS	EN	EN	Partial	3 µa
Sleep-Deep	DIS	EN	EN	RegFile	1.5 µa

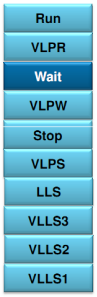
Mode Description and Mode Status –RUN

- Selected after any Reset
- On chip voltage regulator is On, full capability
- Stack pointer (SP), Program Counter(PC) and link register are set
- processor exits reset and reads the start SP
- processor reads the start PC form vector table
- MCG starts in FLL Engages Internal ~ 23 MHz clock
- Reduce power by not setting clock gating bits
- Low Power Boot by setting LPBOOT in FOPT flash location

- **Mode Status:**
  - Run mode is fully operational
  - IDD's from 18ma – 70 ma depending on the frequency.(K)
  - See Errata list for more specifics.

Mode Description and Mode Status – WAIT

Extended Power Modes

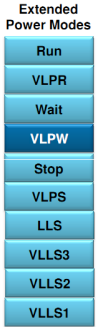


- WAIT – Normal WAIT mode
- core enters Stop (ARM – Sleep) Mode
- INTC/NVIC remains sensitive to interrupts
- Peripherals Continue to be clocked
- Reduce power by clearing clock gating bits in SCGCx
- On interrupt the core exist Stop Mode : Resume processing

- Mode Status:
  - •Wait mode – fully supported
  - •IDD's ~run IDD's minus 5 ma

Mode Description and Mode Status – VLPWait

Extended Power Modes

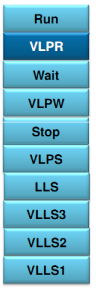


- VLPW – Very Low Power Wait
- core enters Stop (ARM – Sleep) Mode
- INTC/NVIC remains sensitive to interrupts
- On chip voltage regulator is in a mode that supplies only enough power to run the MCU in a reduced frequency
- Bus frequency limited to 2MHz, Flash to 1 MHz
- Reduce power by clearing clock gating bits in SCGCx

- Kinetis Mode Status:
  - •VLPW mode not being supported.
  - •IDD's ~1.0 ma
  - •See Errata list for more specifics.
- •CF+ Mode Status
  - •VLPW fully supported
  - •IDD's ~1.0 ma

Mode Description and Mode Status – VLPRun

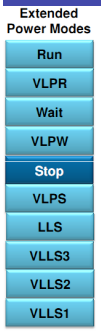
Extended Power Modes



- VLPR - Very Low Power Run
- On chip voltage regulator is in a mode that supplies only enough power to run the MCU in a reduced frequency
- Core and Bus frequency limited to 1Mhz
- Flash frequency limited to 1Mhz
- Reduce power by clearing clock gating bits in SCGCx
- Flash programming and erasing is not allowed.
- FlexMemory (EEPROM) programming is not allowed
- Kinetis Mode Status:
  - •VLPR mode not being supported. It may work with reduce frequencies (core clock ~500 KHz)
  - •IDD's ~1.5 ma
  - •See Errata list for more specifics.
- •CF+ Mode Status:
  - VLPR mode fully supported.
  - IDD's ~1.5 ma
  - You can enter VLPW, STOP, LLS, VLLSx
  - Return to VLPR controlled by LPWUI bit
  - Reduced Frequencies (core clock 2 MHz, Flash 1 MHz)

Mode Description and Mode Status – STOP

Extended Power Modes

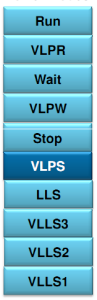


- STOP – Normal STOP mode
- core enters Stop/ DEEPSLEEP Mode
- INTC/NVIC remains sensitive to interrupts
- Platform and peripheral clocks are stopped
- MCG module can be configured to leave reference clocks running
- All SRAM is operating (content retained and I/O states held)

- Mode Status:
  - •STOP mode – fully supported
  - •IDD's ~ 60 ua
  - •Exit from STOP with interrupt
  - •Code execution continues after stop entry(after STOP)
  - •Doesn't need LLWU
  - •If you enter in PEE mode, exit in PBE mode
  - •See Errata with LVD Reset

Mode Description and Mode Status – VLPStop

Extended Power Modes



- VLPS = Very low power Stop
- core enters Stop/ DEEPSLEEP Mode
- INTC/AWIC remains sensitive to interrupts
- Platform and peripheral clock are stopped
- MCG module can be configured to leave reference clocks running
- On chip voltage regulator is in a mode that supplies only enough power to run the MCU in a reduced frequency for recovery to VLPR
- All SRAM is operating (content retained and I/O states held)

- Mode Status:
  - •VLPS mode – fully supported
  - •IDD's ~30 ua
  - •Exit from VLPS with interrupt
  - •Code execution continues after stop entry(after STOP)
  - •Doesn't need LLWU
  - •If you enter in PEE mode, exit in PBE mode

Mode Description and Mode Status – LLS

Extended Power Modes

- LLS = low leakage Stop
- core enters Stop/ DEEPSLEEP Mode
- INTC/NVIC is disabled
- LLWU configured to enable the desire wake up source
- Platform and peripheral clock are stopped
- MCG module can be configured to leave reference clocks running
- All SRAM is retained and I/O states held
- Most of peripheral are in state retention mode (can't operate)
- Functional Modules include LLWU pin wakeup, CMP, TSI, LPT

- Mode Status:
  - •LLS mode – fully supported
  - •IDD's ~10 ua
  - •Exit from LLS with LLWU source, or reset
  - •Fetches LLWU interrupt Vector
  - •WAKEUP bit in SRS set
  - •Code execution continues after stop entry(after stop)
  - •If you enter in PEE mode, exit in PBE mode

Mode Description and Mode Status – VLLS3

Extended Power Modes

- Run
- VLPR
- Wait
- VLPW
- Stop
- VLPS
- LLS
- **VLLS3**
- VLLS2
- VLLS1

- VLLS = Very low leakage Stop3
- core enters Stop/ DEEPSLEEP Mode
- INTC/NVIC is disabled
- LLWU configured to enable the desire wake up source
- Platform and peripheral clock are stopped
- MCG module can be configured to leave reference clocks running
- All SRAM is retained, I/O states held
- Most modules are disabled
- Functional Modules include LLWU pin wakeup, CMP, TSI, LPT

- Mode Status:
  - VLLS3 mode – Fully supported
  - IDD's ~6 ua
  - RAM retained + Register File Module
  - Requires LLWU -Exit with LLWU event, or RESET
  - Recovery from VLLS3 through RESET
  - WAKEUP bit in SRS set
  - If you enter in PEE mode, exit in FEI mode

Mode Description and Mode Status – VLLS2

Extended Power Modes

- Run
- VLPR
- Wait
- VLPW
- Stop
- VLPS
- LLS
- VLLS3
- **VLLS2**
- VLLS1

- VLLS = Very low leakage Stop2
- core enters Stop/ DEEPSLEEP Mode
- INTC/NVIC is disabled
- LLWU configured to enable the desire wake up source
- Platform and peripheral clock are stopped
- MCG module can be configured to leave reference clocks running
- Only partial SRAM is operating (content retained, I/O state held
- Most modules are disabled
- Functional Modules include LLWU pin wakeup, CMP, TSI, LPT

- Mode Status:
  - VLLS2 mode – Fully supported
  - IDD's ~3 ua
  - 4 Kbytes of RAM retained + Register File Module
  - Requires LLWU -Exit with LLWU event, or RESET
  - Recovery from VLLS3 through RESET
  - WAKEUP bit in SRS set
  - If you enter in PEE mode, exit in FEI mode

Mode Description and Mode Status – VLLS1

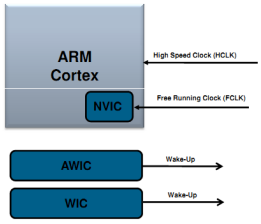
Extended Power Modes

- Run
- VLPR
- Wait
- VLPW
- Stop
- VLPS
- LLS
- VLLS3
- VLLS2
- **VLLS1**

- VLLS = Very low leakage Stop1
- core enters Stop/ DEEPSLEEP Mode
- INTC/NVIC is disabled
- LLWU configured to enable the desire wake up source
- Platform and peripheral clock are stopped
- MCG module can be configured to leave reference clocks running
- NO SRAM is operating (content not retained, I/O state held)
- Most modules are disabled
- Functional Modules include LLWU pin wakeup, CMP, TSI, LPT

- Mode Status:
  - VLLS1 mode – Fully supported
  - IDD's ~1.5 ua
  - Register File Module – No RAM
  - Requires LLWU -Exit with LLWU event, or RESET
  - Recovery from VLLS3 through RESET
  - WAKEUP bit in SRS set
  - If you enter in PEE mode, exit in FEI mode

Cortex low power implementation

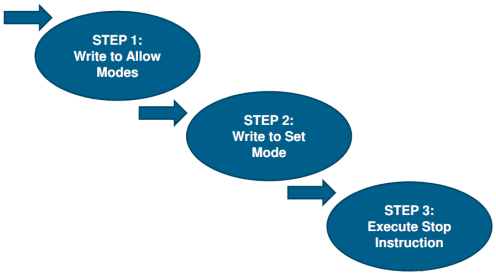


Sleep
- CPU can be clock gated: HCLK = OFF
- NVIC remains sensitive to interrupts: FLCK = ON

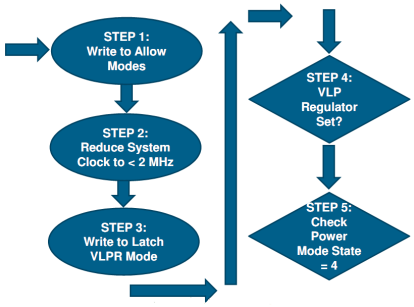
Deep Sleep
- HCLK and FCLK = OFF
- AWIC remains sensitive to selected interrupts
- Cortex-M3 inc. NVIC can be put into state retention

AWIC signals wake-up to PMU
- Cortex core can be woken almost instantaneously
- React to critical external events

Entering Low Power Stop Modes

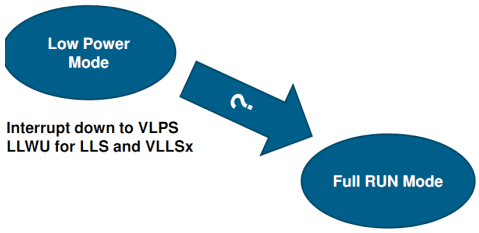


Entering Very Low Power Run Mode



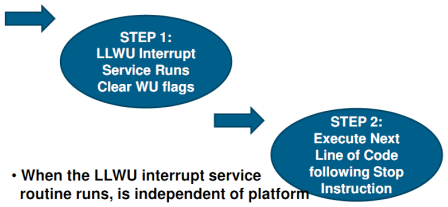
Exiting Low Power Modes

Now that you got into the low power mode …
How do you get out?



Exiting Low Power Modes (LLS)

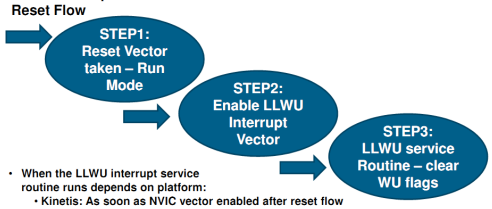
LLWU Wakeup Event



- When the LLWU interrupt service routine runs, is independent of platform
- Kinetis or ColdFire+ MCU wakeup time is about 4 µs

Exiting Low Power Modes (VLLS1, 2 or 3)

LLWU Wakeup Event
Reset Flow



- When the LLWU interrupt service routine runs depends on platform:
  - Kinetis: As soon as NVIC vector enabled after reset flow
  - ColdFire+: As soon as wakeup event occurs and reset vector stacked
  - Kinetis and ColdFire+ MCU VLLS1 wakeup time is about 100 to 140 µs