Augustus Kinzel Uht, Ph.D., P.E.

CURRICULUM VITAE
(as of July 3, 2020)

Contact Information:
44 Torrey Rd.
Cumberland, RI 02864
www.ele.uri.edu/∼uht

Cell: (401) 787-1313
gusuht@gmail.com

Research Interests

Computer Engineering, especially:
Computer architecture: accelerators; Instruction Level Parallelism (ILP); speculative execution; multipath execution; control dependencies, supercomputing.
Adaptive computing: better-than-worst-case design, *viz*: performance maximization; power minimization; environmental, operating and manufacturing conditions' adaptation; use of feedback control systems for adaptation.

Education

8/82 - 12/85 **Ph.D. in Electrical Engineering** (specialization in Computer Engineering), Carnegie-Mellon University, Pittsburgh, PA. Thesis title: *Hardware Extraction of Low-Level Concurrency from Sequential Instruction Streams*. Advisor: Robert G. Wedig.
CONCENTRATIONS: parallel systems, computer architecture and implementation, real-time systems, computer arithmetic.

9/77 - 5/78 **M.Eng.(Elect.)**, Cornell University, Ithaca, NY. Design Project title: *The CLEO Prototype Data Acquisition System*; designed and realized analog and digital system components for a 64,000 analog channel data-acquisition system. Advisor: Nelson H. Bryant.
CONCENTRATIONS: digital systems, analog and digital circuit design, computer architecture, control systems, analog network theory.

9/73 - 5/77 **B.S.** - major in Electrical Engineering, Cornell University, Ithaca, NY.
CONCENTRATIONS: digital systems, analog and digital circuit design, control systems.

Professional Standing and Affiliations

Licensed Professional Engineer in the States of New York, Pennsylvania, and Rhode Island.
Institute of Electrical and Electronics Engineers - Senior Member
Eta Kappa Nu - electrical engineering honor society - member
Sigma Xi - science honor society - member
Association for Computing Machinery - member

Most Relevant Employment and Positions - see following pages for complete accomplishments.

7/2020 on *Retired*

6/2005 - 6/2020 *Professor-in-Residence*. University of Rhode Island, College of Engineering.

2002 - 6/2020 *Member*, *Director* (2002-2009), *Founder*.
URI Microarchitecture Research Insights Laboratory (μRI or MuRI).

1/2014 - 2/2015 *Book Collection Editor*, Computer Engineering Foundations, Currents and Trajectories. Momentum Press, associated with McGraw Hill Education, Professional.

7/01 - 6/05 *Research Professor*. University of Rhode Island, Department of Electrical and Computer Engineering.

1/01 - 6/01 *Adjunct Associate Professor*. Northeastern University, Dept. of Electrical and Computer Engineering.

10/99 - 6/00 *Visiting Scholar*. Northeastern University, Dept. of Electrical and Computer Engineering.

7/98 - 6/01 *Associate Professor* (with tenure). University of Rhode Island, Department of Electrical and Computer Engineering.

6/92 - 6/98 *Assistant Professor*. University of Rhode Island, Department of Electrical and Computer Engineering.

7/86 - 6/92 *Assistant Professor*. University of California, San Diego, Department of Computer Science and Engineering, La Jolla, CA.

1/86 - 5/86 *Visiting Assistant Professor*. Carnegie-Mellon University, Department of Electrical and Computer Engineering, Pittsburgh, PA. Conducted research in computer architecture, and assisted with the teaching and development of an undergraduate computer engineering course. Designed and wrote a real-time software simulator of a microprocessor with an easy-to-use GUI.

1/83 - 12/85 *Graduate Assistant*. Carnegie-Mellon University, Department of Electrical and Computer Engineering, Pittsburgh, PA. Conducted research concerning the performance enhancement of primarily mainframe and super-computers via concurrent and out-of-order execution of code. Supervised undergraduate students in related supporting research projects.

7/78 - 6/82 *Senior Associate Engineer* (10/80 to 6/82), *Associate Engineer* (7/78 to 10/80). International Business Machines Corporation, East Fishkill Facility, Hopewell Jct., NY. Worked on main and extended memory and memory-support systems for large mainframe general-purpose computers. Designed and developed memory array cards and CCD memory system testers.

5/76 - 9/77 *Research Assistant*. Cornell University, Laboratory of Nuclear Studies, Ithaca, NY. Designed and developed the prototype for a computer-controlled large-scale (64,000 channels) analog-data acquisition system.

1/75 - 5/76 *Electronics Technician*. Cornell University, Laboratory of Nuclear Studies, Ithaca, NY. Built, tested, and participated in the development of atomic and sub-atomic particle detectors.

9/74 - 1/75 *Laboratory Technician*. Cornell University, Laboratory of Nuclear Studies, Ithaca, NY. Tested, repaired, and calibrated small-signal amplifiers and their A/D circuitry.

Other Experience (Teaching)

Fall 1983 *Teaching Intern*. Carnegie-Mellon University, Dept. of Electrical and Computer Engineering, Pittsburgh, PA. Assisted in the running of the upper-level undergraduate course: An Introduction to Computer Architecture.

Spring 1978 *Teaching Assistant*. Cornell University, School of Electrical Engineering, Ithaca, NY. Laboratory instructor for an introductory level course in digital logic and design.

Fall 1977 *Teaching Assistant*. Cornell University, School of Electrical Engineering, Ithaca, NY. Laboratory instructor for an upper level and graduate course in semiconductor physics and circuits.

Consulting and Other Part-Time Positions

Consultant, patent litigation, 2002-2003.
Member, Scientific Advisory Board, Parallax Inc., 1988 to 1992.
Consultant, Intel Corporation, Hillsboro, Oregon, Nov., 1990.

Professional Service

Program Committe, 38th IEEE International Conference on Computer Design, (ICCD 2020), Computer Systems Track.
Publications Chair, 2016 IEEE International Symposium on Workload Characterization, IISWC-2016.
Publications Chair, 10th IEEE International Conference on Networking, Architecture, and Storage (NAS 2015).

Program Committee, 5th IEEE International Conference on Networking, Architecture, and Storage (NAS 2010).
Program Committee, Fifth Boston-Area Architecture Workshop, BARC-2007.
Founding Associate Editor, Inderscience International Journal of High Performance Systems Architecture, June 2006 - November 2009.
Organizer (General Chair and Program Chair), Fourth Boston-Area Architecture Workshop, BARC-2006.
Program Committee, International Conference on Parallel and Distributed Systems, 2006.
Associate Editor, Journal of Instruction-Level Parallelism, September 2003 - November 2006.
Review Panel Member and regular *Grant Proposal Reviewer* - National Science Foundation.
Tutorials Chair, 8th High Performance Computer Architecture Conference, February 2002.
Program Committee, First Workshop on Solving the Memory Wall Problem, in conjunction with the 27th International Symposium on Computer Architecture, June 2000.
Founding Member, Member Emeritus, ACM SIGMICRO Website Steering Cmte., 2000 - 2001.
Program Committee, 25th ACM/IEEE International Symposium and Workshop on Microarchitecture (MICRO-25), 1992.
Program Committee, 24th ACM/IEEE International Symposium and Workshop on Microarchitecture (MICRO-24), 1991.
Reviewer: IEEE Computer, IEE Electronics Letters, IEE Proceedings Computers & Digital Techniques, IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, International Symposium on Computer Architecture (ISCA), International Symposium on Microarchitecture (MICRO), High Performance Computer Architecture Conference (HPCA), Electrical and Electronics Engineering Encyclopedia, IEEE Computer Architecture Letters (IEEECAL), International Conference on Parallel and Distributed Systems (ICPADS), IEEE International Parallel & Distributed Processing Symposium (IPDPS), International Conference on Parallel Architectures and Compilation Techniques (PACT), IEEE Transactions on Multi-Scale Computing Systems

Other Honors, Awards, and Scholarships

2001 on	Listed in *Who's Who in America*; various editions.
2013 - 2014	*URI Intellectual Property Recognition Award* - University of Rhode Island.
Apr. 2006	*Best Paper*, architectures track, 20th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2006); see "Refereed Publications"[4].
June 2005	Appointed *Professor-in-Residence*, College of Engineering, University of Rhode Island.
May 2005	Elevated to *Senior Member*, IEEE.
May 12, 2005	*Recognition Award for Outstanding Contributions to Intellectual Property* - University of Rhode Island.
2005 - 2009	Listed in *Who's Who in Science and Engineering*.
2005	Invited Chapters for CRC book; see "Invited Publications"[2, 3].
Mar. 2004	Paper invited for Computer Special Issue; see "Invited Publications"[4].
Sep. 11, 2001	*Second Place* for *Best Paper* in the Work-In-Progress session, Parallel Architectures and Compilation Techniques 2001 Conference; see "Refereed Publications"[15].
May 2, 2001	*Recognition Award for Outstanding Contributions to Intellectual Property* - University of Rhode Island.
June 2000	Paper selected for oral presentation at ASEE 2000 Conference; see "Refereed Publications"[17].
May 2000	Paper invited for IEEE Micro Special Issue; see "Invited Publications"[8].
5/98	*Aurelio Lucci Faculty Excellence Award in Electrical Engineering* - URI Coll. of Engineering.
5/98 - 5/99	*College of Engineering Representative, Sigma Xi Honorary Society, URI Chapter*.
10/27/95	*Panel Member*, First Intel Microprocessor Research Forum, panel discussion topic: "The Future of Microprocessors", Intel Corporation, Santa Clara, CA.
1995	Paper selected to appear in an IEEE Computer Society tutorial (select collection of reprints); see "Refereed Publications"[27].
1989 - 1993	Listed in *Who's Who in the West*.
3/6/87	*Inventor Recognition Award*, Semiconductor Research Corporation.

1/86 *Second Place* for *Best Paper* in the Computer Architecture track, Nineteenth Annual Hawaii International Conference on System Sciences; see "Refereed Publications"[34].
1983 - 1985 Carnegie-Mellon University Graduate Assistantship.
1979 *Informal Award* for memory tester design, International Business Machines, Inc.
1973 - 1977 Cornell Regents Honorary Scholarship.
1973 - 1977 New York State Regents College Scholarship.

Other Service
8/2014 - 1/2017 Rhode Island Association of Conservation Commissions, board member.
12/2013 - 1/2017 Cumberland, RI, Conservation Commission, member.
11/2012 on RI Future, op-ed contributor.
2012 Candidate for Rhode Island State Representative.
2009 on Testified at many RI General Assembly and Cumberland Town Council hearings.
2004 - 2016 IT Asst. Sys. Admin. and general volunteer for various presidential, state and local campaigns.
1980's on Member of several advocacy organizations.

Grants Awarded

Principal Investigator in all cases unless noted otherwise.

From 1995 See Xilinx Corporation Software and Mentor Graphics Corporation Software donations below.

Oct. 26, 2016 Maximizing FPGA Efficiency for Workloads with Arbitrary Granularity (WAG); R. Sendag and A.K. Uht; Intel Corporation; use of high-performance accelerator development system.

April 24, 2002 Hardware Donation for Levo High-ILP Prototype Computer;
Xilinx Corporation; 14 - million-gate-equivalent high-speed FPGA's; list price: $24,010.

May 5, 2001 Hardware Donation for Levo High-ILP Prototype Computer;
Xilinx Corporation; 26 - million-gate-equivalent FPGA's; list price: $31,850.

Dec. 23, 1998 "Advanced Computer Engineering and Science Laboratory (ACES)";
with J. Kowalski, J.-C. Lo, J. Peckham and Q. Yang;
Champlin Foundations; $114,979.

Oct. 21, 1997 Donation of Digital CAD Tools (software);
Xilinx Corporation; originally valued by Xilinx at $60,000; renewable annually; October 1997 - 2000, 2002 on; for both instruction and research.

Oct. 8, 1997 "Equipment for Diverse Computer Architecture Research";
with Q. Yang, J.-C. Lo and D. W. Tufts;
National Science Foundation, #MIP-9729839; $76,730; January 1, 1998 - December 31, 1999.

Aug. 1, 1997 "Order of Magnitude Instruction Level Parallelism";
National Science Foundation, #MIP-9708183; $300,000; July, 1997 - June, 2001.

April 20, 1997 "Equipment for ICED - Integrated Computer Engineering Design Curriculum"; with G. Sadasiv; National Science Foundation, #DUE-9751215; $64,849; July, 1997 - June, 2000.

Nov. 6, 1995 Donation of Digital and Analog CAD Tools (software);
Mentor Graphics Corporation; originally valued by Mentor at $1.3 million; renewable annually; January, 1996 - 2000, 2006 - 2016; for both instruction and research.

Dec. 15, 1994 "Exploiting More Instruction Level Parallelism";
The Intel Corporation; $80,600; December 15, 1994 - December 14, 1997.

June 30, 1994 "Advanced Instruction Level Parallel Processor";
University of Rhode Island, Proposal Development Office; $3,000; July, 1994 - December, 1994.

July 27, 1989 "The Analysis, Measurement and Exploitation of Eager Evaluation in Imperative Instruction Streams"; National Science Foundation Research Initiation Award, #CCR-8910586; $63,438; July, 1989 - June, 1991.

July 1, 1987 "Improving the Performance of both General Purpose and Scientific Computers (a continuation)"; University of California at San Diego Academic Senate Research Grant; $4,217; fiscal 1987/1988.

Nov. 7, 1986 "Improving the Performance of both General Purpose and Scientific Computers"; University of California at San Diego Academic Senate Research Grant; $3,678; fiscal 1986/1987.

Conference Panel Membership

Oct. 27, 1995 Panel discussion topic: "The Future of Microprocessors"
First Intel Microprocessor Research Forum, Intel Corporation, Santa Clara, CA.

Web Notable

Nov. 28, 2009 "HyperText Markup Language" talk; at: ele.uri.edu/∼uht/talks/html/html.htm
No. 1 hit of about 1,040,000,000 for Google search of: *html talk*

Extramural Talks Presented

Feb. 27, 2008 "TEAtime: Timing Error Avoidance for Performance Enhancement and Environment & Process Adaptation," with live hardware demonstration;
Brown University, Providence, Rhode Island.

"Levo: A Scalable Processor With High IPC" presented at:
Apr. 30, 2003 University of Rochester, Rochester, NY.
Apr. 28, 2003 IBM Research, Yorktown Heights, NY.
Apr. 15, 2003 University of Virginia.

"TEAtime: Timing Error Avoidance for Performance Enhancement and Environment Adaptation," with live hardware demonstration, presented at:
Apr. 30, 2003 University of Rochester, Rochester, NY.
Apr. 28, 2003 IBM Research, Yorktown Heights, NY.
Apr. 24, 2003 University of California, Los Angeles.
Apr. 23, 2003 University of California, San Diego.
Apr. 21, 2003 Intel Research, Santa Clara, CA.
Apr. 15, 2003 University of Virginia.
Apr. 9, 2003 Cornell University.
Apr. 4, 2003 Villanova University, Villanova, PA.
Feb. 28, 2003 Sun Microsystems, Burlington, MA.

Nov. 19, 1999 "DEE & Levo: ILP Speedups in the 10's (& 100's?)"
Northeastern University, Boston, MA.

June 30, 1997 "Verification of ILP Speedups in the 10's for Disjoint Eager Execution"
Intel Corporation, Portland, OR.

Oct. 22, 1996 "ILP Speedups in the 10's"
Brown University, Providence, RI.

Oct. 26, 1995 "ILP Speedups in the 10's"
First Intel Microprocessor Research Forum,
Intel Corporation, Santa Clara, CA.

July 24, 1995 "ILP Speedups in the 10's"
Intel Corporation, P6 (Pentium Pro) Architecture Group, et al, Portland, OR.

June 1, 1990 "Desirable Code Transformations for a Concurrent Machine /
Understanding Eager Evaluation of Imperative Instruction Streams"
IBM Research Division, Yorktown Heights, New York.

July 22, 1988 "The Reduction of Branch Effects",
Gould Computer Systems, San Diego, CA.

August, 1987 "Incremental Performance Contributions of Hardware Concurrency Extraction Techniques",
University of Illinois at Urbana-Champaign, Center for Supercomputing Res. and Dev.

March, 1987 "Hardware Extraction of Low-Level Concurrency from Sequential Instruction Streams",
San Diego Supercomputer Center, La Jolla, CA.

(Talks also given at almost all conferences listed below.)

Invited Publications

[1] Sendag, R., Yilmazer, A., Yi, J., and Uht, A. K. The Impact of Wrong-Path Memory References in Cache-Coherent Multiprocessor Systems. *Journal of Parallel and Distributed Computing*, 67 (2007):1256–1269, March 24 2007. Special Issue on Best Papers in 2006 IEEE International Parallel and Distributed Processing Symposium.

[2] Morano, D. A., Kaeli, D. R., and Uht, A. K. Resource Flow Microarchitectures. In *Speculative Execution in High Performance Computer Architectures, Boca Raton, FL, USA*, pages 393–419. CRC Press, May 2005. Invited chapter.

[3] Uht, A. K. Multipath Execution. In *Speculative Execution in High Performance Computer Architectures, Boca Raton, FL, USA*, pages 135–160. CRC Press, May 2005. Invited chapter.

[4] Uht, A. K. Going Beyond Worst-Case Specs with TEAtime. *Computer*, 37(3):51–56, March 2004. Invited paper for Special Issue on "Better Than Worst-Case Design".

[5] Uht, A. K. Teradactyl: an Easy-to-Use Supercomputer. In *Proceedings of the International Symposium of Santa Caterina on Challenges in the Internet and Interdisciplinary Research (SSCCII-2004), Amalfi, Italy*. IPSI, January-February 2004. Invited and refereed paper.

[6] Uht, A. K. Uniprocessor Performance Enhancement Through Adaptive Clock Frequency Control. In *Proceedings of the SSGRR-2003w International Conference on Advances in Infrastructure for e-Business, e-Education, e-Science, e-Medicine, and Mobile Technologies on the Internet, L'Aquila, Italy*. Telecom Italia, January 6-12, 2003. Invited and refereed paper.

[7] Uht, A. K., Langford, S., and Morano, D. Interactive High-Performance Processor Understanding via the Web. In *Proceedings of the SSGRR 2002w International Conference on Advances in Infrastructure for e-Business, e-Education, e-Science, and e-Medicine on the Internet, L'Aquila, Italy*. Telecom Italia, January 21-27, 2002. LevoVis paper.

[8] Uht, A. K., Lo, J.-C., Sun, Y., Daly, J. C., and Kowalski, J. Building Real Computer Systems. *IEEE MICRO*, 20(3):48–56, May-June 2000. Invited and refereed paper, Special Issue on Computer Architecture Education.

[9] Uht, A. K. The Integrated Computer Engineering Design (ICED) Curriculum. In *Proceedings of the 1998 Workshop on Computer Architecture Education, held in conjunction with the 25th International Symposium on Computer Architecture*, June 1998.

[10] Uht, A. K. Desirable Code Transformations for a Concurrent Machine. In *Languages and Compilers for Parallel Computing*, pages 511–530. MIT Press, 1990. Invited chapter.

[11] Vin, H. M. and Uht, A. K. Dynamic Instruction Substitution: A Technique of Minimizing Data Dependencies for Memory References. *IEEE-CS TC-MICRO MICROARCH Newsletter*, 4(1 and 2), July 1989. Invited paper.

[12] Uht, A. K., Polychronopoulos, C. D., and Kolen, J. F. On the Combination of Hardware and Software Concurrency Extraction Methods. In *Proceedings of the Twentieth Annual Workshop on Microprogramming (MICRO-20)*, pages 133–141, December 1987.

Refereed Publications

[1] Cavus, M., Shatnawi, M., Sendag, R., and Uht, A. Prefetching, Pre-Execution and Branch Outcome Streaming for In- Memory Database Lookups. In *BARC 2020 Boston Area Architecture Workshop, Boston, MA, USA*, 2020.

[2] Cavus, M., Shatnawi, M., Sendag, R., and Uht, A. Exploring Prefetching, Pre-Execution and Branch Outcome Streaming for In-Memory Database Lookups. *IEEE Computer Architecture Letters*, 18(02), December, 2019.

[3] Uht, G. Lets Keep it to Ourselves: Dont Disclose Vulnerabilities. *Computer Architecture Today, ACM SIGARCH*, January 31, 2019. https://www.sigarch.org/lets-keep-it-to-ourselves-dont-disclose-vulnerabilities/.

[4] Sendag, R., Yilmazer, A., Yi, J., and Uht, A. K. Quantifying and Reducing the Effects of Wrong-Path Memory References in Cache-Coherent Multiprocessor Systems. In *Proceedings of the 20th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2006), Rhodes Island, Greece.* IEEE, April 25-29, 2006. One of four Best Papers out of 531 submissions.

[5] Uht, A. K. TEAtime Adaptive-Computing Case-Study, Demonstration and Updated Results. In *2nd Workshop on Architecture Research using FPGA Platforms (WARFP-2006), held in conjunction with the 12th International Symposium on High-Performance Computer Architecture (HPCA-12), Austin, Texas, USA*, February 12, 2006. Accepted, was to appear; withdrawn due to illness.

[6] Uht, A. K. ILP is Dead, Long Live IPC! In *Proceedings of the Fourth Boston-Area Architecture Workshop (BARC 2006), Kingston, RI, USA*, February 3, 2006.

[7] Yilmazer, A., Sendag, R., Yi, J., and Uht, A. K. Investigating the Effects of Wrong-Path Memory References in Shared-Memory Multiprocessor Systems. In *Proceedings of the Fourth Boston-Area Architecture Workshop (BARC 2006), Kingston, RI, USA*, February 3, 2006.

[8] Uht, A. K. and Vaccaro, R. J. TEAPC: Temperature Adaptive Computing in a Real PC. In *Proceedings of the Second Workshop on Temperature-Aware Computer Systems (TACS-2), ISCA, Madison, WI, USA*. IEEE and ACM, June 5, 2005.

[9] Uht, A. K. Uniprocessor Performance Enhancement through Adaptive Clock Frequency Control. *IEEE Transactions on Computers*, 54(2):132–140, February 2005.

[10] Uht, A. K. and Vaccaro, R. J. TEAPC: Adaptive Computing and Underclocking in a Real PC. In *Proceedings of the First IBM $P=ac^2$ Conference, Yorktown Heights, NY, USA*, pages 45–54. IBM T.J. Watson Research Center, October 6-8, 2004. Talk presented with live hardware demonstration.

[11] Uht, A. K., Morano, D., Khalafi, A., and Kaeli, D. R. Levo - A Scalable Processor With High IPC. *The Journal of Instruction-Level Parallelism*, 5, August 2003. (http://www.jilp.org/vol5).

[12] Morano, D., Khalafi, A., Kaeli, D. R., and Uht, A. K. Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture. *ACM SIGARCH Computer Architecture Newsletter*, March 2003.

[13] Uht, A., Khalafi, A., Morano, D., Alba, M. d., and Kaeli, D. Realizing High IPC Using Time-Tagged Resource Flow Computing. In *Proceedings of the Euro-Par 2002 Conference, Paderborn, Germany*, pages 490–499. ACM, IFIP, August 28, 2002.

[14] Morano, D., Khalafi, A., Kaeli, D. R., and Uht, A. K. Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture. In *Proceedings of the Workshop On Chip Multiprocessors: Processor Architecture and Memory Hierarchy Related Issues (MEDEA2002), at PACT 2002, Charlottesville, Virginia, USA*, September 22, 2002. Also appears in ACM SIGARCH Computer Architecture Newsletter, March 2003.

[15] Uht, A. K., Khalafi, A., Morano, D., Wenisch, T., de Alba, M., and Kaeli, D. Levo: IPC in the 10's via Resource Flow Computing. *IEEE TCCA Newsletter, Special Issue*, December 2001. Presented at PACT 2001 Work-In-Progress (WIP) Session, September 2001.

[16] Wenisch, T., Swaszek, P. F., and Uht, A. K. Combined Error Correcting and Compressing Codes. In *Proceedings of the 2001 IEEE International Symposium on Information Theory (ISIT 2001), Washington, DC*, June 2001.

[17] Uht, A. K. The URI Integrated Computer Engineering Design (ICED) Curriculum: Progress Report. In *Proceedings of the ASEE 2000 Annual Conference, St. Louis, MO*, June 2000.

[18] Uht, A. K. The Integrated Computer Engineering Design (ICED) Curriculum. *IEEE Technical Committee on Computer Architecture Newsletter*, pages 5–7, February 1999. Special Issue on Computer Architecture Education.

[19] Uht, A. K. and Sun, Y. The Laboratory Environment of the URI Integrated Computer Engineering Design (ICED) Curriculum. In *Proceedings of the Frontiers in Education Conference, Tempe, Arizona*, pages 331–336, November 1998.

[20] Uht, A. K. The Integrated Computer Engineering Design (ICED) Curriculum. In *Proceedings of the 4th Annual Workshop on Computer Architecture Education, held in conjunction with the Fourth High Performance Computer Architecture Conference*, January 1998.

[21] Uht, A. K. Use of CAD Tools in the Integrated Computer Engineering Design (ICED) Curriculum. In *Proceedings of the 14th International Conference of the Mentor Graphics Users' Group, Portland, OR*, October 1997.

[22] Uht, A. K., Sindagi, V., and Somanathan, S. Branch Effect Reduction Techniques. *IEEE COMPUTER*, 30(5):71–81, May 1997.

[23] Uht, A. K. and Sindagi, V. Disjoint Eager Execution: An Optimal Form of Speculative Execution. In *Proceedings of the 28th International Symposium on Microarchitecture (MICRO-28), Ann Arbor, MI*, pages 313–325, November/December 1995.

[24] Uht, A. K. and Johnson, D. B. Data Path Issues in a Highly Concurrent Machine. In *Proceedings of the Twenty-Fifth International Symposium on Microarchitecture, MICRO-25*, pages 115–118. ACM-IEEE, December 1992.

[25] Uht, A. K. Requirements for Optimal Execution of Loops with Tests. *IEEE Transactions on Parallel and Distributed Systems*, 3(5):573–581, September 1992.

[26] Uht, A. K. Concurrency Extraction via Hardware Methods Executing the Static Instruction Stream. *IEEE Transactions on Computers*, 41(7):826–841, July 1992.

[27] Uht, A. K. A Theory of Reduced and Minimal Procedural Dependencies. *IEEE Transactions on Computers*, 40(6):681–692, June 1991. Also appears in the tutorial "Instruction-Level Parallel Processors", Torng, H.C., and Vassiliadis, S., Eds., IEEE Computer Society Press, 1995, pages 171-182.

[28] Wang, S. S. H. and Uht, A. K. Ideograph/Ideogram: Framework/Architecture for Eager Evaluation. In *Proceedings of the 23rd Annual Symposium and Workshop on Microprogramming and Microarchitecture, MICRO-23*, pages 125–134, November 1990.

[29] Wang, S. S. H. and Uht, A. K. Program Optimization with Ideograph. In *Proceedings of the 1989 International Conference on Parallel Processing*, volume II, pages 153–159, August 1989.

[30] Jacobs, J. H., Uht, A. K., and Ord, R. C. Modelling the Effects of Instruction Queue Loading on a Static Instruction Stream Micro-Architecture. In *Proceedings of the 21st Annual Workshop on Microprogramming and Microarchitecture, San Diego, CA, USA*, pages 11–20. ACM-IEEE, November 1988.

[31] Uht, A. K. Requirements for Optimal Execution of Loops with Tests. In *Proceedings of the International Conference on Supercomputing, St. Malo, France*, pages 230–237, July 4-8, 1988.

[32] Uht, A. K. Incremental Performance Contributions of Hardware Concurrency Extraction Techniques. In *Proceedings of the International Conference on Supercomputing, Athens, Greece*, pages 355–376, June 1987. Springer-Verlag Lecture Note Series.

[33] Uht, A. K. and Wedig, R. G. Hardware Extraction of Low-level Concurrency from Serial Instruction Streams. In *Proceedings of the International Conference on Parallel Processing*, pages 729–736, August 1986.

[34] Uht, A. K. An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code. In *Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences*, pages 41–50, January 1986.

[35] Neves, F. and Uht, A. K. Memory Error Correction without ECC. *IBM Technical Disclosure Bulletin*, 24(7A):3471, December 1981.

[36] Aichelmann, F. J., Fehn, T. P., and Uht, A. K. Interlaced Data/Regeneration for Memory Refresh. *IBM Technical Disclosure Bulletin*, 24(1B):489–490, June 1981.

Patents - Issued

[1] Uht, A. K., Morano, D., and Kaeli, D. Not-taken path instruction for selectively generating a forwarded result from a previous instruction based on branch outcome. USA Patent No. 8,601,245. Issued: December 3, 2013.

[2] Uht, A. K., Morano, D., and Kaeli, D. Concurrent execution of instructions in a processing system. USA Patent No. 7,991,980. Issued: August 2, 2011.

[3] Uht, A. K. System und verfahren zur leistungsverbesserung digitaler systeme. Germany Patent No. 60334837. Issued: December 16, 2010.

[4] Sendag, R., Yilmazer, A., and Uht, A. K. System and method for cache replacement. USA Patent No. 7,721,048. Issued: May 18, 2010.

[5] Uht, A. K. System and Method of Digital System Performance Enhancement. European Union Patent No. 03790151.9. Issued: October 2, 2009.

[6] Uht, A. K. System and Method of Digital System Performance Enhancement. USA Patent No. 7,555,084. Issued: June 30, 2009.

[7] Uht, A. K., Morano, D., and Kaeli, D. Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates. USA Patent No. 7,409,534. Issued: August 5, 2008.

[8] Uht, A. K., Morano, D., and Kaeli, D. Automatic and transparent hardware conversion of traditional control flow to predicates. USA Patent No. 7,380,108. Issued: May 27, 2008.

[9] Uht, A. K., Morano, D., and Kaeli, D. Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates. USA Patent No. 7,210,025. Issued: April 24, 2007.

[10] Uht, A. K. System and Method of Digital System Performance Enhancement. USA Patent No. 6,985,547. Issued: January 10, 2006.

[11] Uht, A. K., Morano, D., and Kaeli, D. Resource Flow Computing Device. USA Patent No. 6,976,150. Issued: December 13, 2005.

[12] Uht, A. K. System and Method of Digital System Performance Enhancement. World (non-USA) patent source document No. WO2004051907A3, October 28, 2004.

[13] Uht, A. K. System for Extracting Low-Level Concurrency from Serial Instruction Streams. USA Patent No. 5,201,057. Issued: April 6, 1993.

Refereed-or-Invited Abstracts and Posters

[1] Kadin, M., Reda, S., and Uht, A. K. Central vs. distributed dynamic thermal management for multi-core processors: which one is better? In *Proceedings of the 19th ACM Great Lakes Symposium on VLSI, Boston, MA, USA*, pages 137–140. ACM, May 10-12, 2009. Extended abstract and poster.

[2] Uht, A. K. Adaptive Computing and ILP Intellectual Property of A.K. Uht. In *URI Research Week, Kingston, RI*, October, 2005. Invited poster.

[3] Uht, A. K. and Vaccaro, R. J. Adaptive Computing. In *Proceedings of the Third Annual Boston Architecture Conference (BARC-2005), Brown University, Providence, RI, USA*, January 21 2005. Talk presented with live hardware demonstration.

[4] Uht, A. K. The URI Integrated Computer Engineering Design (ICED) Curriculum: Progress Report. In *ASEE 2000 Annual Conference, St. Louis, MO*, June 2000. Poster presentation.

[5] Uht, A. K. and Johnson, D. B. Data Path Issues in a Highly Concurrent Machine. In *Proceedings of the 19th International Symposium on Computer Architecture, Gold Coast, Australia*, page 431. ACM/IEEE, May 1992. Abstract. Poster presented at conference.

[6] Vin, H. M. and Uht, A. K. Integrated Approach to Concurrent Code Execution with respect to Instruction Scheduling and Memory Reference Disambiguation. In *Supercomputing '89, Reno, Nevada*. ACM/IEEE, November 1989. Poster presented.

Other Publications

[1] Uht, A. K. TEAxx Prototype Series Documentation. Technical Report 20050215-1, Microarchitecture Research Institute, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, February 15, 2005.

[2] Uht, A. K. and Vaccaro, R. J. TEAPC: Adaptive Computing and Underclocking in a Real PC. Technical Report 20041027-1, Microarchitecture Research Institute, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, October 27, 2004.

[3] Uht, A. K. TEAtime Prototype Thermal System. Technical Report 20031110-1, Microarchitecture Research Institute, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, November 11, 2003.

[4] Uht, A. K. TEAtime Prototype VCCInt Documentation. Technical Report 20030911-1, Microarchitecture Research Institute, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, September 11, 2003.

[5] Uht, A. K. TEAtime Prototype System Hardware. Technical Report 20031013-1, Microarchitecture Research Institute, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, October 13, 2003.

[6] Uht, A. K. TEAtime Prototype Oscillator, Version 2.0. Technical Report 20031006-1, Microarchitecture Research Institute, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, October 6, 2003.

[7] Uht, A. K. TEAtime Prototype Oscillator, Version 1.0. Technical Report 20030915-1, Microarchitecture Research Institute, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, October 6, 2003.

[8] Morano, D., Khalafi, A., Kaeli, D. R., and Uht, A. K. Implications of Register and Memory Temporal Locality for Distributed Microarchitectures. Technical report, Dept. of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA, October 2002.

[9] Uht, A. K., Morano, D., Khalafi, A., and Kaeli, D. Levo - A Scalable Billion Transistor CPU With High IPC. Technical Report 082002-1000, Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881-0805, August 2002.

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[11] Uht, A. K. Disjoint Eager Execution: What It Is / What It Is Not. *ACM SIGARCH Computer Architecture News*, 30(1), March 2002.

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[15] Wenisch, T. and Uht, A. K. HDLevo - VHDL Modeling of Levo Processor Components. Technical Report 072001-100, Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, July 20, 2001.

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[17] Uht, A. K. High Performance Memory System for High ILP Microarchitectures. Technical Report 0797-0002, Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, August 26, 1997.

[18] Uht, A. K. Overview of the Levo High-ILP Computer. Technical Report 0797-0001, Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, August 26, 1997.

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[21] Uht, A. K. Extraction of Massive Instruction Level Parallelism. *ACM SIGARCH Computer Architecture News*, 21(1 and 3):(June) 5–12, March and June 1993.

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[23] Uht, A. K. and Johnson, D. B. Data Path Issues in a Highly Concurrent Machine. Technical Report CS92-262, Department of Computer Science and Engineering, University of California, San Diego, La Jolla, CA, September 1992. An extended paper.

[24] Uht, A. K. and Wang, S. S. Understanding Eager Evaluation of Imperative Instruction Streams, Part 1. Technical Report CS90-171, Department of Computer Science and Engineering, University of California, San Diego, La Jolla, CA, May 1990.

[25] Uht, A. K. Notes on a Theory of Minimal Procedural Dependencies. Technical Report CS90-165, Department of Computer Science and Engineering, University of California, San Diego, La Jolla, CA, USA, February 1990.

[26] Uht, A. K. Concurrency Extraction via Hardware Methods Executing the Static Instruction Stream - an extended paper. Technical Report CS89-144, Department of Computer Science and Engineering, University of California, San Diego, La Jolla, CA, USA, January 1989.

[27] Wang, S. S. and Uht, A. K. Ideograph and Minimal Procedural Dependencies. Technical Report CS88-140, Department of Computer Science and Engineering, University of California, San Diego, La Jolla, CA, USA, December 1988.

[28] Uht, A. K. Hierarchical Computation Server: Goals, Architecture, and Issues. Technical Report CS88-119, Department of Computer Science and Engineering, University of California, San Diego, La Jolla, CA, USA, November 1987.

[29] Uht, A. K. *Hardware Extraction of Low-Level Concurrency from Sequential Instruction Streams*. PhD thesis, Electrical and Computer Engineering, Carnegie-Mellon University, Pittsburgh, December 1985. Available from University Microfilms International, Ann Arbor, Michigan, U.S.A.

[30] Uht, A. K. Exploitation of Low-Level Concurrency: an Implementation and Architecture. Technical Report CMUCAD-85-52, Department of Electrical and Computer Engineering, Carnegie-Mellon University, Pittsburgh, PA, May 1985.

URI Non-Research Activities - July 1992 on

Professional Development

- Faculty Teaching Fellow - one year

Semester Courses Taught

Lower Division - Microprocessor Laboratory - taught 6 times

Upper Division - Digital Computer Design - taught 8 times
- Introduction to Computer Architecture - taught twice

Graduate - Instruction Level Parallelism and the Ubiquitous, Bothersome Branch - taught 3 times
- Graduate Seminar - taught 3 times

Semester Courses Created or Heavily Revised

Upper Division - Digital Computer Design
- Introduction to Computer Architecture

Graduate - Instruction Level Parallelism and the Ubiquitous, Bothersome Branch

Committee and Service Work

2013 - 2016 Aided Dean of Engineering with new Engineering Center funding - state bond issues.
2009 - 2012 Intellectual Property Policy development.
2007 - 2009 Department faculty evaluator.
2007 - 2009 Department tenure advisor, two faculty members.
2003 - 2009 Mentor for junior computer engineering faculty.
1992 - 2007 Faculty Search Committee - member or consultant
1999 - 2001 Faculty Marshal

2000 Undergraduate Computer Engineering program - Coordinator
5/98 - 9/99 Administrator Evaluation Committee for Dean Thomas Kim, Engineering - member
9/97 - 12/00 Computer Engineering (ICED) Laboratory Equipment - Co-ordinator & Designer
7/96 Computer Systems Manager Search Committee - member
7/95 - 9/99 Computer Engineering CAD Tools Committee - member
Obtained CAD tool donation from Mentor Graphics
7/94 - 9/99 Computer Engineering Curriculum Committee - member
Heavily revised undergraduate curriculum; obtained its approval at all University levels
Obtained major equipment funding for the new curriculum from the NSF - w/Prof. Sadasiv
7/92 - 6/93 Computer Engineering Committee - member
7/92 - 6/97 Undergraduate Student Advisor for Computer Engineering Majors
7/92 - 6/93 Graduate Computer Engineering Advisor

Student Project or Thesis Advisor

Ph.D. thesis committee chairman: 2 students.
Ph.D. thesis committee member: 4 students.
Master's thesis committee chairman: 4 students.
Master's thesis committee member: 2 students.
Master's project advisor: 3 students.
Undergraduate projects: 6 students.

UCSD Non-Research Activities - July 1986 to June 1992

Quarter Courses Taught

Lower Division - Scientific Application of Computers - taught 2 times
Upper Division - Introduction to Digital Logic - taught 1 time
- Digital System Concepts and Design - taught 5 times
Graduate - Principles in Computer Architecture, Part 1 - taught 6 times
- Principles in Computer Architecture, Part 2 - taught 6 times
- Graduate Seminar on Instruction Level Parallelism - taught 2 times

Quarter Courses Created or Heavily Revised

Upper Division - Digital System Concepts and Design
Graduate - Principles in Computer Architecture, Parts 1 & 2

Committee and Service Work

7/91 - 6/92 M.S. Student Advisor in CSE Dept.
7/88 - 1/90 Computer Engineering Advisory Committee of the Division of Engr. - Chairman
Began development of Computer Engr. Graduate Program of CSE and ECE Depts.
7/88 - 1/90 Computer Engineering Committee of the CSE Dept. - Chairman
7/87 - 7/88 Computer Committee of the UCSD Academic Senate - member
7/86 - 6/92 Undergraduate Student Advisor for Computer Engineering Majors
7/86 - 1/90 Computer Engineering Advisory Committee of the Division of Engr. - Member
Helped develop revised Computer Engineering Major curriculum

Student Project or Thesis Advisor

Ph.D. thesis committee chairman: 2 students.
Ph.D. thesis committee member: 3 students.
Master's thesis committee chairman: 1 student.
Master's projects or equivalent: 15 students.
Undergraduate projects: 21 students.