TEAtime Adaptive-Computing Case-Study, Demonstration and Updated Results

Augustus K. Uht
Microarchitecture Research Institute
Dept. of Electrical and Computer Engineering
University of Rhode Island
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1 Case Study

The TEAtime system described herein was prototyped and characterized in a matter of days after the TEAtime idea was conceived. This rapid-prototyping was only possible by using an FPGA.

TEAtime (Timing Error Avoidance) is a microarchitectural/logic/analog design that allows any digital system to 'maximize' its performance under any given environmental, operating or manufacturing conditions [4, 6, 7]. It is a form of *adaptive computing*. Variations on its current design can be used to 'minimize' power usage or to 'optimize' operation based on some combination of performance and power usage. TEAtime was conceived in the latter part of 2002.

The key TEAtime idea is to use a "tracking logic" circuit that mimics the structure and wiring of the system's critical delay path (with an added small safety-margin delay); see Figure 1. This tracking logic is subject to the same conditions as the original logic of the system; that is, if the original logic's delay goes down due to a decrease in temperature, the delay of the tracking logic also decreases. By incorporating the tracking logic in a simple feedback loop including a variable frequency oscillator driving the overall system clock, the system clock frequency and hence performance increase. The clock is repeatedly sped up until an error is detected in the tracking logic, but before any errors have occurred in the real logic. The clock speed is then reduced until the error disappears, and then the process repeats.

The simplicity of the basic TEAtime design suggested that it would be possible to prototype a significant digital system utilizing TEAtime. Ideally, the digital system used in the prototype would be a CPU, so as to demonstrate TEAtime's worth and functionality on a realistically complex system.

Prohibitive cost, time and labor constraints precluded creating the entire system on a custom chip. Further, commercial PCs were not an option since their complexity might well mask the basic worth of the TEAtime ideas (see: [8-10] for a recent application of TEAtime to PCs). While FPGAs had been widely available for some time, their densities at reasonable costs were low (a 100,000 or so gate-equivalents per device), and few if any suitable canned IPs for existing processors were available.

Fortunately, in one of those lovely cases of teaching/research symbiosis, I had previously designed a 32-bit 5-stage pipelined CPU w/forwarding for use in a computer architecture course. I also had an assembler available for this CPU. The CPU's ISA is simple. An equivalent of a one-cycle-access unified L1 cache was also included on the FPGA. The resulting computer fit into an existing Xilinx FPGA, the 100,000 gate-equivalent Spartan II XC2S100, which was part of a COTS (Commercial Off-The-Shelf) prototyping board, the XESS XSA-100. I added a small external Voltage-Controlled Oscillator to complete the basic TEAtime system. For experimental and control purposes, I also added a programmable power supply used only for the FPGA, and appropriate control software running on a standard PC. The PC is connected to the FPGA via a standard PC legacy parallel interface. See Figure 2 for a picture of the final prototype system.

After the system assembly/construction and testing, TEAtime worked immediately, and in the flesh. (As an aside, for an engineer this is a real high!) Characterization and performance data were quickly obtained from the experimental apparatus, and the work was published within a few months [3].

I was able to go from the basic TEAtime idea to its first operation in a matter of days. The key components allowing such a fast turnaround time were the FPGA, its Xilinx and Mentor Graphics design tools and an existing CPU design (it had been already been tested in an FPGA simulation).

In the Spring of 2003 I took the TEAtime prototype around the country, including a live TEAtime demo in a standard 'hour'-long talk. TEAtime worked perfectly at all of the presentations (about 10 of them; see my CV [5] for a list of the talk venues). (It also survived about 20 passes through airport security scanners; be still, my heart.)

The TEAtime work has been published and patented [3, 4, 6, 7]. (Figures 1 & 2 appeared in [4].)

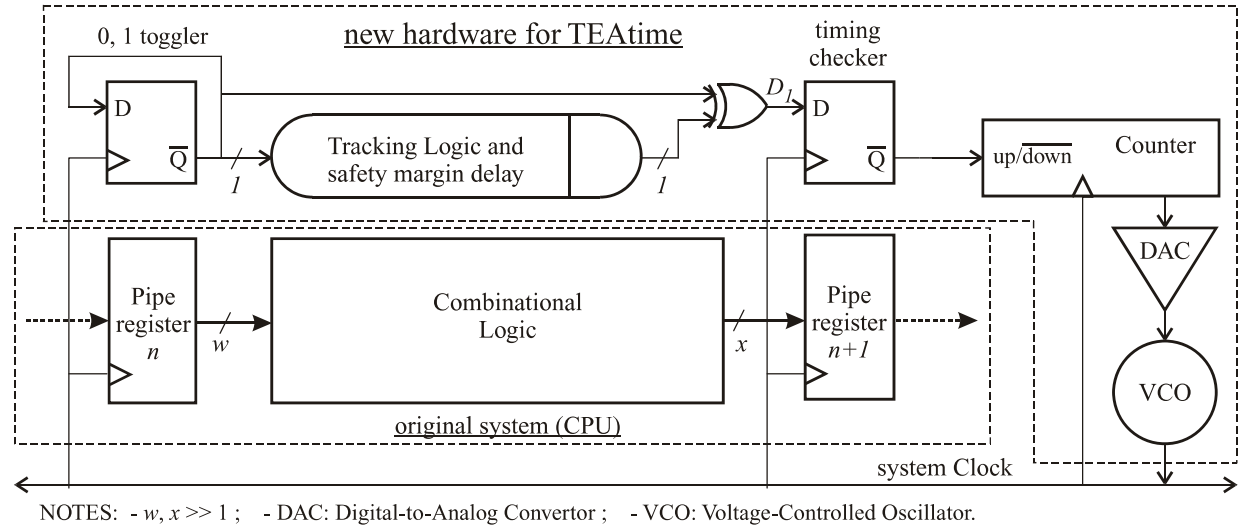

Figure 1. TEAtime modified system: the basic structure used to dynamically adapt the system to its environment and 'maximize' performance. 'Minimization' of power is possible with a modified design.

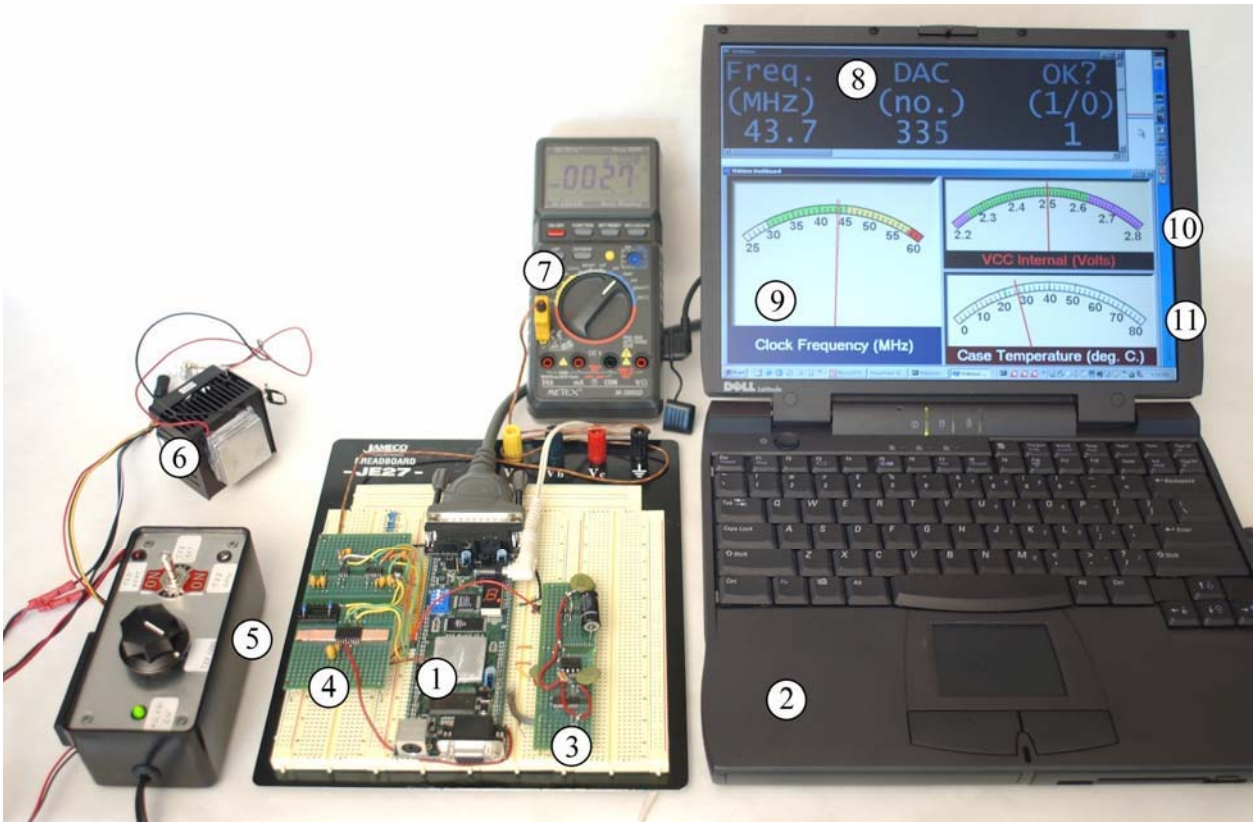

Figure 2. Prototype system. ***Legend:***
1. FPGA and XESS XSA-100 prototype card
2. PC host
3. Custom oscillator card with DAC and VCO
4. Custom card containing the PC host-controlled FPGA internal supply voltage
5. Custom thermoelectric device controller
6. Thermoelectric device assembly
7. FPGA case temperature meter
8. Controller program command-line window and data display
9. System clock frequency meter
10. VCCint meter
11. FPGA case temperature meter

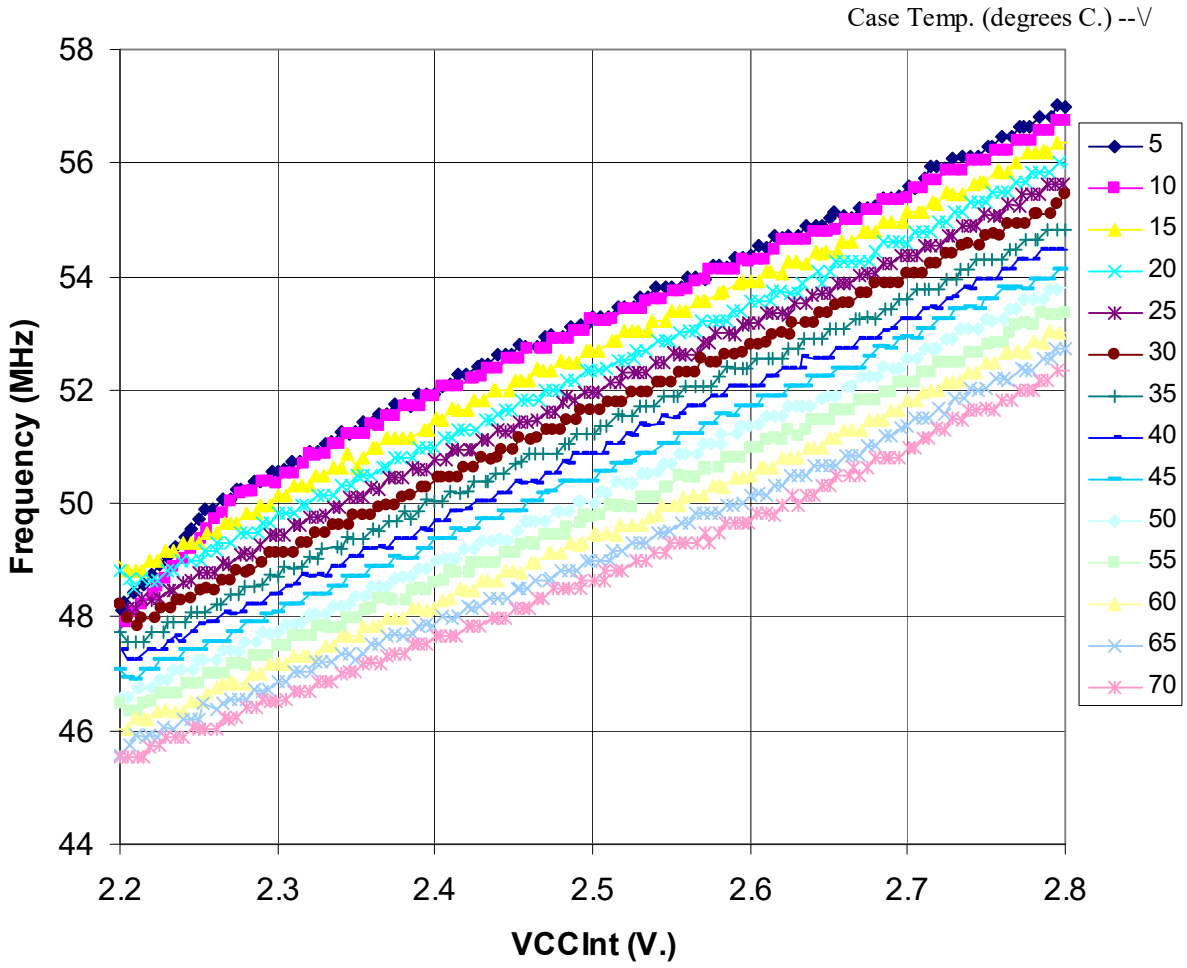

Figure 3. System clock frequency as a function of both supply voltage (VCCint) and case temperature. VCCint and temperature are both independent variables, while the clock frequency is a dependent variable. TEAtime successfully adapts to varying environmental and operating conditions. The system uses tuned tracking logic. The baseline frequency is 30 MHz, assuming classical worst-case path techniques. Therefore with a tuned system TEAtime is able to achieve a performance gain of 90%, almost a factor of two.

2 Demonstration

I propose to demonstrate the TEAtime prototype at the Workshop. While I am not sure exactly what the allowable parameters of demonstrations are at the Workshop, there are many possibilities, depending on the interests of the Workshop Organizers and/or the audience. Demonstrations can be interactive.

Some possibilities are:

1. Basic operation and adaptivity.
2. Performance 'maximization.'
3. Operation with varying temperature.
4. Operation with varying supply voltage.
5. Limits of operation.

The demonstration setup is shown in Figure 2. Note that the (host) PC's video output can be connected to a standard video projector (best with a resolution of 1024 x 768, i.e., XGA). The prototype can therefore be demonstrated in any kind of lecture venue.

Variable temperatures are created via the use of a Peltier device: it generates a temperature difference between two plates, dependent on the sign and magnitude of an applied DC voltage. The effect of a changing temperature is also effectively demonstrated by putting an ice cube on top of the FPGA chip. (No joke, I did this at every venue visited in 2003. I cheat by first putting the ice cube in a plastic zip-lock freezer bag.) This tends to get the attention of the audience.

Given the short lengths of the talks (15 minutes and 5 minutes), I think the prototype demonstration is best left for the poster session. I am happy to work with the Organizers to devise something suitable for whatever will fit the Organizers' desires and Workshop's constraints, within reason.

3 Updated Results

As previously mentioned, the TEAtime work has been published, with one exception: the best results were not published in detail.

The initial measurements assumed a very conservative tracking logic design. With a large safety-margin delay the gain in performance was about 50%. After the tracking logic was tuned by reducing the safety-margin delay, the measurements were repeated; the performance gain increased to almost 2x; see Figure 3.

4 Summary

TEAtime is a simple idea and is readily applied to any existing digital system design. TEAtime's functionality and attributes have been demonstrated in a prototype. Other approaches often require very careful and complex component design[1], or are costly[2]. The performance differences among all three approaches are not clear, may be workload-dependent; this is an open research topic.

The two key components allowing TEAtime's rapid prototyping and characterization were an FPGA and a COTS system containing the FPGA. With current FPGA gate densities much more complex processors or other digital designs could be operated in a TEAtime fashion for demonstration or production purposes, or to augment other microarchitectural research such as that in [11].

The TEAtime idea is sound and can lead to large improvements in performance, as well as allowing a digital system to adapt to existing conditions. As such, a TEAtime system may often work in conditions too severe for classically-designed systems to operate, e.g., in a desert. Conversely, TEAtime can take advantage of typical or better than typical conditions and operate faster than the norm.

An engaging and flexible live demonstration of the TEAtime prototype is possible at the Workshop.

More recent results further illustrate TEAtime's worth. Performance gains of almost two times a conventionally-designed system have been demonstrated.

References

[1] D. Ernst, N. S. Kim, S. Das, S. Pant, R. Rao, T. Pham, C. Ziesler, D. Blaauw, T. Austin, K. Flautner, and T. Mudge, "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," in *Proc. of the 2003 Int'l Symp. on Microarchitecture*. San Diego, Calif., USA: IEEE, ACM, Dec. 2003.

[2] A. K. Uht, "Achieving Typical Delays in Synchronous Systems via Timing Error Toleration," Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, Technical Report 032000-0100, March 10, 2000. Available via **http://www.ele.uri.edu/~uht**.

[3] A. K. Uht, "Uniprocessor Performance Enhancement Through Adaptive Clock Frequency Control," in Proc. of the SSGRR-2003w Int'l Conf. on Advances in Infrastructure for e-Business, e-Education, e-Science, e-Medicine, and Mobile Technologies on the Internet. L'Aquila, Italy: Telecom Italia, January 6-12, 2003.

[4] A. K. Uht, "Going Beyond Worst-Case Specs with TEAtime," *Computer*, vol. 37, no. 3, pp. 51-56, March 2004. Special Issue on ``Better Than Worst-Case Design".

[5] Curriculum Vitae of A.K. Uht, Dec. 25, 2005. URL: **http://www.ele.uri.edu/~uht/bio/cv.pdf**.

[6] A. K. Uht, "Uniprocessor Performance Enhancement through Adaptive Clock Frequency Control," *IEEE Transactions on Computers*, vol. 54, no. 2, pp. 132-140, February 2005.

[7] A. K. Uht, "System and Method of Digital System Performance Enhancement," U.S. Patent No. 6,985,547. Issued: January 10, 2006.

[8] A. K. Uht and R. J. Vaccaro, "TEAPC: Adaptive Computing and Underclocking in a Real PC," in *Proc. of the First IBM P=ac^2 Conference*. Yorktown Heights, NY, USA: IBM T.J. Watson Research Center, October 6-8, 2004, pp. 45-54.

[9] A. K. Uht and R. J. Vaccaro, "Adaptive Computing," in *Proc. of the Third Annual Boston-area Architecture Conference (BARC-2005)*. Brown University, Providence, RI, USA, Jan. 21 2005.

[10] A. K. Uht and R. J. Vaccaro, "TEAPC: Temperature Adaptive Computing in a Real PC," in *Proc. of the Second Wksp. on Temperature-Aware Computer Systems (TACS-2), ISCA*. Madison, WI, USA: June 5, 2005.

[11] S. Velusamy, W. Huang, J. Lach, M. Stan, and K. Skadron, "Experiences Using FPGAs for Temperature-Aware Microarchitecture Research," in *Proc. of the Wrkshp. on Architecture Research using FPGA Platforms, held at HPCA-11*. San Francisco, CA, USA, Feb. 2005.