1. ( ) Which of the state diagrams on the right corresponds to the timing diagram shown below? The state is labeled as \((y_1y_0)\).

(E) none of the above.

2. ( ) For the above problem, given the initial state \((y_1y_0) = 01\) and a new waveform for the input \(X\), select the correct progression of the state.

(E) none of the above.

3. ( ) The state diagram shown on the right is implemented with three JK flip-flops. The state is labeled as \((y_2y_1y_0)\), where \(y_1\) is the output of the flip-flop with input \(J_1\) and \(K_1\), etc. States 110 and 111 do not appear and can be treated as don't-care states. After simplification, which of the following is the correct logic in the next state decoder for driving \(K_1\)? Hint: Just focus on the state variable \(y_1\). Don't spend time solving the entire system. \(K_1 = \) (A) \(y_2y_1\), (B) \(y_0\), (C) 1, (D) \(T \cdot (y_1 + y_0)\). (E) none of the above.

4. ( ) For the above problem, which of the following mnemonic Karnaugh maps is correct for \(J_1\)?

(E) none of the above.

5. ( ) Which of the following statements is not correct? (A) Dynamic RAM provides a cost-effective way to pack a huge amount of memory cells onto a small chip. (B) Static RAM must be refreshed frequently to preserve the content of the memory. (C) PROM can be programmed once by the user but cannot be reprogrammed. (D) EEPROM can be erased using an electrical circuit and reprogrammed over and over again. (E) none of the above.
6. ( ) A read-only memory (ROM) and two D flip-flops are used to implement a state machine, which has two state variables \((y_1, y_0)\), an input \(X\), and an output \(Y\). The state diagram is shown below. The ROM has 3 address lines \((a_2, a_1, a_0)\). Each address contains 3 data bits \((d_2, d_1, d_0)\). Which of the following shows the correct content of the ROM?

\[
\begin{array}{ccc|ccc|ccc}
\text{00} & \text{01} & \text{10} & \text{11} & \text{CLK} & \text{Y} & \text{X} & \text{D}_1 & \text{D}_0 \\
\hline
\text{000} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\text{001} & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
\text{010} & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
\text{011} & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\
\text{100} & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\text{101} & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
\text{110} & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
\text{111} & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\
\end{array}
\]

(E) none of the above.

7. ( ) For the above problem, if we use a programmable logic array (PLA) instead of the ROM to implement the state machine, which of the following PLA’s is correct?

(A) \(y_1 y_0 X \rightarrow D_1 D_0 Y\)

(B) \(y_1 y_0 X \rightarrow D_1 D_0 Y\)

(C) \(y_1 y_0 X \rightarrow D_1 D_0 Y\)

(D) \(y_1 y_0 X \rightarrow D_1 D_0 Y\)

(E) none of the above.

8. ( ) For the above problem, what’s the correct logic for the output? Note that the output is \(Y\), or \(d_0\) from the PLA.

(E) \(Y = a_2 a_1\), (B) \(Y = a_1 a_0\), (C) \(Y = a_2 a_0\), (D) \(Y = a_2 a_1 + a_1 a_0\),

(F) none of the above.

(E) none of the above.